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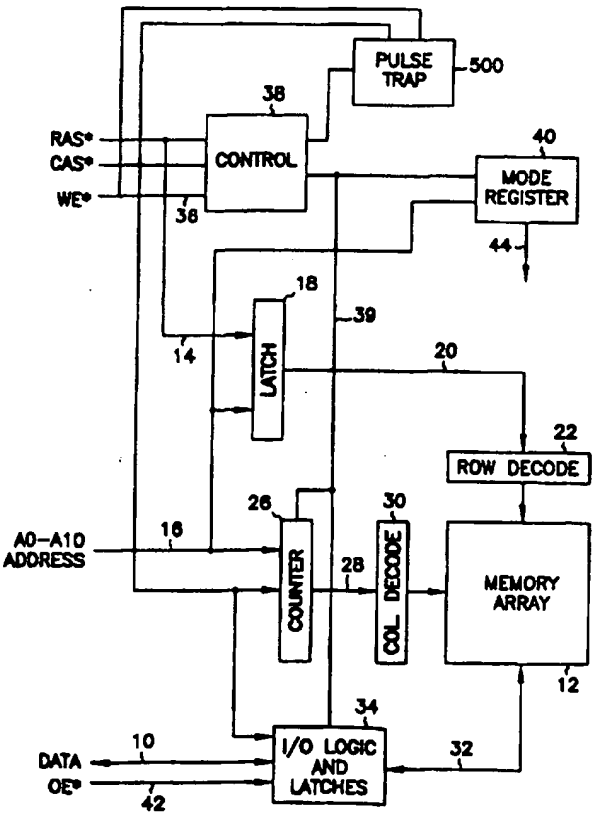
(54) Title: BURST EDO MEMORY DEVICE

(57) Abstract

An integrated circuit memory device is designed for high speed data access and for compatibility with existing memory systems. An address strobe signal is used to latch a first address. During a burst access cycle the address is incremented internal to the device with additional address strobe transitions. A new memory address is only required at the beginning of each burst access. Read/Write commands are issued once per burst access eliminating the need to toggle the Read/Write control line at the device cycle frequency. Transitions of the Read/Write control line during a burst access will terminate the burst access, reset the burst length counter and intialize the device for another burst access. A two stage pipelined output buffer latches read data in a first stage while data from a second stage is driven from the device. Internal read lines may become invalid in preparation for additional access cycles after the data is latched in the first stage. The device is compatible with existing Extended Data Out DRAM device pinouts, Fast Page Mode and Extended Data Out Single In-Line Memory Module pinouts, and the other memory circuit designs. The memory device maintains compatibility with nonburst mode devices such as Extended Data Out (EDO) and Fast Page Mode through bond option or mode selection circuitry. A multiplexer selects between the input address and the burst address generator output to feed an asynchronous address transition detection circuit. The address transition detection circuit generates an equilibration control signal between memory access cycles.



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BURST EDO MEMORY DEVICE

FIELD OF THE INVENTION

This invention relates to memory device architectures designed to provide high density data storage with high speed read and write access cycles.

BACKGROUND OF THE INVENTION

Dynamic Random Access Memory devices (DRAMs) are among the highest volume and most complex integrated circuits manufactured today. Except for their high volume production, the state of the art manufacturing requirements of these devices would cause them to be exorbitantly priced. Yet, due to efficiencies associated with high volume production, the price per bit of these memory devices is continually declining. The low cost of memory has fueled the growth and development of the personal computer. As personal computers have become more advanced, they in turn have required faster and more dense memory devices, but with the same low cost of the standard DRAM. Fast page mode DRAMs are the most popular standard DRAM today. In fast page mode operation, a row address strobe (/RAS or RAS*) is used to latch a row address portion of a multiplexed DRAM address. Multiple occurrences of the column address strobe (/CAS or *CAS) are then used to latch multiple column addresses to access data within the selected row. On the falling edge of /CAS an address is latched, and the DRAM outputs are enabled. When /CAS transitions high the DRAM outputs are placed in a high impedance state (tri-state). With advances in the production of integrated circuits, the internal circuitry of the DRAM operates faster than ever. This high speed circuitry has allowed for faster page mode cycle times. A problem exists in the reading of a DRAM when the device is operated with minimum fast page mode cycle times. /CAS may be low for as little as 15 nanoseconds, and the data access time from /CAS to valid output data (tCAC) may be up to 15 nanoseconds; therefore, in a worst case scenario there is no time to latch the output data external to the memory device. For devices that operate faster than the specifications require, the data may still only be valid for a few nanoseconds. On a heavily loaded microprocessor memory bus, trying to

latch an asynchronous signal that is valid for only a few nanoseconds is very difficult. Even providing a new address every 35 nanoseconds requires large address drivers which create significant amounts of electrical noise within the system. To increase the data throughput of a memory system, it has been common practice to place multiple devices on a common bus. For example, two fast page mode DRAMs may be connected to common address and data buses. One DRAM stores data for odd addresses, and the other for even addresses. The /CAS signal for the odd addresses is turned off (high) when the /CAS signal for the even addresses is turned on (low). This interleaved memory system provides data access at twice the rate of either device alone. If the first /CAS is low for 20 nanoseconds and then high for 20 nanoseconds while the second /CAS goes low, data can be accessed every 20 nanoseconds or 50 megahertz. If the access time from /CAS to data valid is fifteen nanoseconds, the data will be valid for only five nanoseconds at the end of each 20 nanosecond period when both devices are operating in fast page mode. As cycle times are shortened, the data valid period goes to zero.

There is a demand for faster, higher density, random access memory integrated circuits which provide a strategy for integration into today's personal computer systems. In an effort to meet this demand, numerous alternatives to the standard DRAM architecture have been proposed. One method of providing a longer period of time when data is valid at the outputs of a DRAM without increasing the fast page mode cycle time is called Extended Data Out (EDO) mode. In an EDO DRAM the data lines are not tri-stated between read cycles in a fast page mode operation. Instead, data is held valid after /CAS goes high until sometime after the next /CAS low pulse occurs, or until /RAS or the output enable (/OE or OE*) goes high. Determining when valid data will arrive at the outputs of a fast page mode or EDO DRAM can be a complex function of when the column address inputs are valid, when /CAS falls, the state of /OE and when /CAS rose in the previous cycle. The period during which data is valid with respect to the control line signals (especially /CAS) is determined by the specific implementation of the EDO mode, as adopted by the various DRAM

manufacturers.

Methods to shorten memory access cycles tend to require additional circuitry, additional control pins and nonstandard device pinouts. The proposed industry standard synchronous DRAM (SDRAM)for example has an additional pin for receiving a system clock signal. Since the system clock is connected to each device in a memory system, it is highly loaded, and it is always toggling circuitry in every device. SDRAMs also have a clock enable pin, a chip select pin and a data mask pin. Other signals which appear to be similar in name to those found on standard DRAMs have dramatically different functionality on a SDRAM. The addition of several control pins has required a deviation in device pinout from standard DRAMs which further complicates design efforts to utilize these new devices. Significant amounts of additional circuitry are required in the SDRAM devices which in turn result in higher device manufacturing costs.

In order for existing computer systems to use an improved device having a nonstandard pinout, those systems must be extensively modified. Additionally, existing computer system memory architectures are designed such that control and address signals may not be able to switch at the frequencies required to operate the new memory device at high speed due to large capacitive loads on the signal lines. The Single In-Line Memory Module (SIMM) provides an example of what has become an industry standard form of packaging memory in a computer system. On a SIMM, all address lines connect to all DRAMs. Further, the row address strobe (/RAS) and the write enable (/WE or *WE) are often connected to each DRAM on the SIMM. These lines inherently have high capacitive loads as a result of the number of device inputs driven by them. SIMM devices also typically ground the output enable (/OE) pin making /OE a less attractive candidate for providing extended functionality to the memory devices.

There is a great degree of resistance to any proposed deviations from the standard SIMM design due to the vast number of computers which use SIMMs. Industry's resistance to radical deviations from the standard, and the inability of current systems to accommodate the new memory devices will

delay their widespread acceptance. Therefore only limited quantities of devices with radically different architectures will be manufactured initially. This limited manufacture prevents the reduction in cost which typically can be accomplished through the manufacturing improvements and efficiencies associated with a high volume product.

It is desirable to design and manufacture a memory device having a standard DRAM pinout and a burst mode of operation where multiple data values can be sequentially written to or read from the device in response to a single address location and multiple access cycle strobes. It is also desirable that this new memory device operate at higher frequencies than standard DRAMs.

In a standard DRAM device, equalization of internal data I/O lines is performed in response to column address transitions in preparation for reading or writing data from another memory cell, and also in response to a receipt of a write command to reduce the maximum signal transition on the data lines once the write drivers are enabled. Since there is a relatively wide time period in which column addresses may become valid, it has been advantageous to use an asynchronous address transition detection circuit to generate an equilibration control signal in response to address transitions. In EDO and fast page mode devices for example, the column address is treated as valid during a page mode cycle while /CAS is high. A read cycle will begin while /CAS is high at the column address indicated by the column address input signals. However, the column address is allowed to change until /CAS falls. Any column address change during the /CAS high time will require a new equilibration of I/O lines and the selection of the new column. When /CAS falls, the column address is latched and further transitions are masked. Equilibration of I/O lines allows for faster sensing of read data, and for faster writing of input data. If the data lines are each equalized to one half of Vcc for example, then the write data drivers will only need to drive one line from half Vcc to ground, and the other from half Vcc to Vcc. Otherwise, if the write data is not equal to the data previously on the I/O lines, the write data drivers will need to drive both true and compliment I/O

lines a full Vcc swing for each data bit being written. Equalization of the data I/O lines reduces the maximum write cycle time by eliminating the worst case signal swing conditions. A similar situation exists during read cycles. In a read cycle, data sense amplifiers only need to drive an equilibrated I/O line from half Vcc to Vcc or ground. If the I/O lines were not equilibrated, the sense amplifiers would need to be large enough to overcome the full data signals on the I/O lines in a read cycle in a short period of time to allow for fast data access. A simple method of equilibrating the I/O lines is to: disable I/O line drivers; isolate the I/O lines from the digit lines; and couple complimentary I/O lines together. When a true I/O line is coupled to a complimentary I/O line, a logic high will be coupled to a logic low and each line will equalize to a potential approximately half way between a high and a low. It is important to disable the I/O line drivers during equilibration to prevent a true logic driver from being coupled to a complimentary logic driver which will draw excessive current from the logic high source to the logic low source.

In a burst access memory device, each access cycle can begin at a fixed point in time relative to the access cycle strobe or clock signal. In this case, an asynchronous address detection circuit is not required since address changes can be restricted to a fixed point in time relative to the access cycle strobe.

SUMMARY OF THE INVENTION

An integrated circuit memory device with a standard DRAM pinout is designed for high speed data access and for compatibility with existing memory systems. A high speed burst mode of operation is provided where multiple sequential accesses occur following a single column address, and read data is output relative to the /CAS control signal. In the burst mode of operation the address is incremented internal to the device eliminating the need for external address lines to switch at high frequencies. Read/Write commands are issued once per burst access eliminating the need to toggle the Read/Write control line at high speeds. Only one control line per memory chip (/CAS) must toggle at the operating frequency in order to clock the

internal address counter and the data input/output latches. The load on each /CAS is typically less than the load on the other control signals (/RAS, /WE and /OE) since each /CAS typically controls only a byte width of the data bus. A data output buffer has a two stage pipeline mode of operation which allows for further speed increases by latching read data in an intermediate data latch, and allowing internal read signals to precharge prior to latching the data in an output latch and driving the data from the part. Internal circuitry of the memory device is largely compatible with existing Extended Data Out (EDO) DRAMs. This similarity allows the two part types to be manufactured on one die with a limited amount of additional circuitry. The ability to switch between a standard non-burst mode and a high speed burst mode allows the device to be used to replace standard devices, and eliminates the need to switch to more complex high speed memory devices. Internal address generation provides for faster data access times than is possible with either fast page mode or EDO DRAMs. This high speed operation eliminates the need to interleave memory devices in order to attain a high data throughput. In contrast to the 50 megahertz interleaved memory system described above, the output data from this device will be valid for approximately 15 nanoseconds significantly easing the design of circuitry required to latch the data from the memory. Operating frequencies significantly higher than 50 megahertz are possible with this architecture due to internal address generation, pipelined read circuitry, an extended valid data output period, and a single lightly loaded control signal operating at the operating frequency or one half of the operating frequency. The device is compatible with existing memory module pinouts including Single In-Line Memory Module (SIMM), Multi-Chip Module (MCM) and Dual In-Line Memory Module (DIMM) designs. This combination of features allows for significant system performance improvements with a minimum of design alterations.

A single integrated circuit die has both burst mode access and page mode access capabilities. In page mode operation, the equilibrate signal is generated asychronously in response to column address transitions while /CAS is high. In burst mode, the equilibrate control signal is generated

synchronously in response to /CAS transitions which control the generation of burst addresses. A multiplexer is used to direct the input address or the burst address to the address transition detection circuit. Among other benefits, use of the asynchronous address transition detection circuit in the burst mode eliminates the requirement for a synchronous equilibration control signal generation circuit, and minimizes the impact of the burst address path on the optimized asynchronous address path. In operation, at the beginning of a burst access, the initial burst address is fed through the asynchronous address path to the address transition detection circuit to generate an equilibrate signal, then the address path is switched to the burst address generator. At the beginning of each access cycle within the burst access the burst address will generate an equilibrate signal through the address transition detection circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the invention as well as objects and advantages will be best understood by reference to the appended claims, detailed description of particular embodiments and accompanying drawings where:

Figure 1 is an electrical schematic diagram of a memory device in accordance with one embodiment of the invention;

Figure 2 is a table showing linear versus interleaved addressing formats;

Figure 3 is a pinout of the memory device of Figure 1;

Figure 4 is a timing diagram for a method of accessing the device of Figure 1;

Figure 5 is a further timing diagram for accessing the device of Figure 1;

Figure 6 is an electrical schematic diagram of an output buffer circuit in accordance with the teachings of the present invention;

Figure 7 is a schematic diagram of a specific embodiment of the output buffer circuit of Figure 6;

Figure 8 is a timing diagram of the operation of the circuit of Figure 7;

Figure 9 is block level schematic of a data path portion of the device

of Figure 1;

Figure 10 is a more detailed schematic of a portion of the circuitry of Figure 9;

Figure 11 is schematic diagram of a portion of the column address path of the device of Figure 1;

Figure 12 is an alternate schematic diagram of a portion of the column address path of the device of Figure 1;

Figure 13 is another alternate schematic diagram of a portion of the column address path of the device of Figure 1;

Figure 14 is a pulse trapping circuit of Figure 1;

Figure 15a is a high transition latch of the circuit of Figure 14;

Figure 15b is a timing diagram of the circuit of Figure 15a;

Figure 15c is a logic table of the timing diagram of Figure 15b:

Figure 16a is a low transition latch of the circuit of Figure 14;

Figure 16b is a timing diagram of the circuit of Figure 16a;

Figure 16c is a logic table of the timing diagram of Figure 16b:

Figure 17 is a timing diagram of the circuit of Figure 14.

Figure 18 is a schematic diagram of a computer system designed in accordance with the teachings of the present invention;

Figure 19 is an electrical schematic diagram of a Single In-Line Memory Module in accordance with another embodiment of the invention:

Figure 20 is a front view of a Single In-Line Memory Module designed in accordance with the teachings of this invention;

Figure 21 is a table of the pin numbers and signal names of the Single In-Line Memory Module of Figure 20; and

Figure 22 is a timing diagram of a burst memory not including the features of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 is a schematic representation of a sixteen megabit device designed in accordance with the present invention. The device is organized as a 2Meg x 8 burst EDO DRAM having an eight bit data input/output path 10 providing data storage for 2,097,152 bytes of information in the memory array

12. The device of Figure 1 has an industry standard pinout for eight bit wide EDO DRAMs. An active-low row address strobe (/RAS) signal 14 is used to latch a first portion of a multiplexed memory address, from address inputs A0 through A10 16, in latch 18. The latched row address 20 is decoded in row decoder 22. The decoded row address is used to select a row of the memory array 12. A column address strobe (/CAS) signal 24 is used to latch a second portion of a memory address from address inputs 16 into column address counter 26. The latched column address 28 is decoded in column address decoder 30. The decoded column address is used to select a column of the memory array 12.

In a burst read cycle, data within the memory array located at the row and column address selected by the row and column address decoders is read out of the memory array and sent along data path 32 to output latches 34. Data 10 driven from the burst EDO DRAM may be latched external to the device in synchronization with /CAS after a predetermined number of /CAS cycle delays (latency). For a two cycle latency design, the first /CAS falling edge is used to latch the initial address for the burst access. The first burst data from the memory is latched in an intermediate latch shortly after it becomes valid on internal data lines. The data from the intermediate data latch is then latched in the output latch and driven from the memory after the second /CAS falling edge, and remains valid through the third /CAS falling edge. Latching the data in an intermediate latch allows for access cycles to begin immediately after each /CAS low transition. Once the memory device begins to output data in a burst read cycle, the output drivers 34 will continue to drive the data lines without tri-stating the data outputs during /CAS high intervals dependent on the state of the output enable and write enable (/OE and /WE) control lines, thus allowing additional time for the system to latch the output data. Once a row and a column address are selected, additional transitions of the /CAS signal are used to advance the column address within the column address counter in a predetermined sequence. The time at which data will be valid at the outputs of the burst EDO DRAM is dependent only on the timing of the /CAS signal provided that /OE is maintained low, and

/WE remains high. The output data signal levels may be driven in accordance with standard CMOS, TTL, LVTTL, GTL, or HSTL output level specifications.

The address may be advanced linearly, or in an interleaved fashion for maximum compatibility with the overall system requirements. Figure 2 is a table which shows linear and interleaved addressing sequences for burst lengths of 2,4 and 8 cycles. The "V" for starting addresses A1 and A2 in the table represent address values that remain unaltered through the burst sequence. The column address may be advanced with each /CAS transition, each pulse, or multiple of /CAS pulses in the event that more than one data word is read from the array with each column address. When the address is advanced with each transition of the /CAS signal, data is also latched in the intermediate latch, latched in the output latch and driven from the part after each /CAS transition. In this case, the device latency is referenced to each edge of the /CAS signal. This allows for a burst access cycle where the highest switching control line (/CAS) toggles only once (high to low or low to high) for each memory cycle. This is in contrast to standard DRAMs which require /CAS to go low and then high for each cycle, and synchronous DRAMs which require a full clock cycle (high and low transitions) for each memory cycle. For maximum compatibility with existing EDO DRAM devices, the invention will be further described in reference to a device designed to latch and advance a column address on falling edges of the /CAS signal. For designs where falling edges of the /CAS signal initiate an access cycle, the falling edge may be said to be the active transition of the /CAS signal.

It may be desirable to latch and increment the column address after the first /CAS falling edge in order to apply both the latched and incremented addresses to the array at the earliest opportunity in an access cycle. For example, a device may be designed to access two data words per cycle (prefetch architecture). The memory array for a prefetch architecture device may be split into odd and even array halves. The column address least significant bit is then used to select between odd and even halves while the

other column address bits select a column within each of the array halves. In an interleaved access mode with column address 1, data from columns 0 and 1 would be read and the data from column 1 would be output followed by the data from column 0 in accordance with standard interleaved addressing as described in SDRAM specifications. In a linear access mode column address 1 would be applied to the odd array half, and incremented to address 2 for accessing the even array half to fulfill the two word access. One method of implementing this type of device architecture is to provide a column address incrementing circuit between the column address counter and the even array half. The incrementing circuit would increment the column address only if the initial column address in a burst access cycle is odd, and the address mode is linear. Otherwise the incrementing circuit would pass the column address unaltered. For a design using a prefetch of two data accesses per cycle, the column address would be advanced once for every two active edges of the /CAS signal. Prefetch architectures where more than two data words are accessed are also possible.

Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access may require more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory will approach one access per cycle, but the data out of the memory may be offset by a number of cycles due to the pipeline length and/or the desired latency from /CAS.

In the burst access memory device, each new column address from the column address counter is decoded and is used to access additional data within the memory array without the requirement of additional column addresses being specified on the address inputs 16. This burst sequence of data will continue for each /CAS falling edge until a predetermined number of data accesses equal to the burst length has occurred. A /CAS falling edge received after the last burst address has been generated will latch another column address from the address inputs 16 and a new burst sequence will begin. Read data is latched and output with each falling edge of /CAS after the first /CAS latency.

For a burst write cycle, data 10 is latched in input data latches 34. Data targeted at the first address specified by the row and column addresses is latched with the /CAS signal when the first column address is latched (write cycle data latency is zero). Other write cycle data latency values are possible; however, for today's memory systems, zero is preferred. Additional input data words for storage at incremented column address locations are latched by /CAS on successive /CAS pulses. Input data from the input latches 34 is passed along data path 32 to the memory array where it is stored at the location selected by the row and column address decoders. As in the burst read cycle previously described, a predetermined number of burst access writes will occur without the requirement of additional column addresses being provided on the address lines 16. After the predetermined number of burst writes has occurred, a subsequent /CAS pulse will latch a new beginning column address, and another burst read or write access will begin.

The memory device of Figure 1 may include the option of switching between burst EDO and standard EDO modes of operation. In this case, the write enable signal /WE 36 may be used at the row address latch time (/RAS falling, /CAS high) to determine whether memory accesses for that row will be burst or page mode cycles. If /WE is low when /RAS falls, burst access cycles are selected. If /WE is high at /RAS falling, standard extended data out (EDO) page mode cycles are selected. Both the burst and EDO page mode cycles allow for increased memory device operating frequencies by not requiring the data output drivers 34 to place the data lines 10 in a high impedance state between data read cycles while /RAS is low. DRAM control circuitry 38, in addition to performing standard DRAM control functions, controls the I/O circuitry 34 and the column address counter/latch 26 in accordance with the mode selected by /WE when /RAS falls. For EDO page mode cycles, the intermediate data latch is bypassed in the output buffer circuitry and data is latched directly in the output latch. In a burst mode only DRAM, or in a device designed with an alternate method of switching between burst and non-burst access cycles, the state of /WE when /RAS falls may be used to switch between other possible modes of operation such as

interleaved versus linear addressing modes.

The write enable signal is used in burst access cycles to select read or write burst accesses when the initial column address for a burst cycle is latched by /CAS. /WE low at the column address latch time selects a burst write access. /WE high at the column address latch time selects a burst read access. The level of the /WE signal must remain high for read and low for write burst accesses throughout the burst access. A low to high transition within a burst write access terminates the burst access, preventing further writes from occurring. A high to low transition on /WE within a burst read access likewise terminates the burst read access and places the data output 10 in a high impedance state. Transitions of the /WE signal may be locked out during critical timing periods within an access cycle in order to reduce the possibility of triggering a false write cycle, and/or to guarantee the completion of a write cycle once it has begun. After the critical timing period the state of /WE determines whether a burst access continues, is initiated, or is terminated.

In a standard burst access memory device, the WE* signal required a minimum pulse width defined by time T_{BTH} following the rising edge of CAS* to terminate a burst access. For a memory not including the present invention, Figure 22 illustrates both the minimum pulse width T_{BTH}, and a WE* low pulse 31 which is less that T_{BTH}. After the critical timing period, the state of WE* is used to determine whether a burst access continues, is initiated, or is terminated. A minimum write enable pulse width is only required when it is desired to terminate a burst read and then begin another burst read, or terminate a burst write prior to performing another burst write with a minimum delay between burst accesses.

Termination of a burst access places the DRAM in a state to receive another burst access command. Both /RAS and /CAS going high during a burst access also terminates the burst access cycle placing the data drivers in a high impedance output state. Read data may remain valid at the device outputs if /RAS alone goes high while /CAS is active for compatibility with hidden refresh cycles, otherwise /RAS high alone may be used to terminate a burst access. A minimum write enable pulse width is only required when it is

desired to terminate a burst read and then begin another burst read, or terminate a burst write prior to performing another burst write with a minimum delay between burst accesses. In the case of burst reads, /WE transitions from high to low to terminate a first burst read, and then /WE transitions back high prior to the next falling edge of /CAS in order to specify a new burst read cycle. For burst writes, /WE transitions high to terminate a current burst write access, then back low prior to the next falling edge of /CAS to initiate another burst write access. A minimum /WE pulse width may be specified to guarantee recognition of the /WE pulse despite /WE lockout periods. If no /WE lockout circuit is used, termination of a burst access may be edge sensitive to the /WE signal.

A basic implementation of the device of Figure 1 may include a fixed burst length of 4, a fixed /CAS latency of 2 and a fixed interleaved sequence of burst addresses. This basic implementation requires very little additional circuitry to the standard EDO page mode DRAM, and may be mass produced to provide the functions of both the standard EDO page mode and burst EDO DRAMs. This device also allows for the output enable pin (/OE) to be grounded for compatibility with many SIMM module designs. When not disabled (tied to ground), /OE is an asynchronous control which will prevent data from being driven from the part in a read cycle if it is inactive (high) prior to /CAS falling and remains inactive beyond /CAS rising. If these setup and hold conditions are not met, then the read data may be driven for a portion of the read cycle. It is possible to synchronize the /OE signal with /CAS, however this would typically increase the /CAS to data valid delay time and doesn't allow for the read data to be disabled prior to /RAS high without an additional /CAS low pulse which would otherwise be unnecessary. In a preferred embodiment, if /OE transitions high at any time during a read cycle the outputs will remain in a high impedance state until the next falling edge of /CAS despite further transitions of the /OE signal.

Programmability of the burst length, /CAS latency and address sequences may be accomplished through the use of a mode register 40 which latches the state of one or more of the address input signals 16 or data signals

10 upon receipt of a write-/CAS-before-/RAS (WCBR) programming cycle. In such a device, outputs 44 from the mode register control the required circuits on the DRAM. Burst length options of 2, 4, 8 and full page as well as /CAS latencies of 1, 2 and 3 may be provided. For a latency of 1, the intermediate data latch is bypassed. For a latency of 3, an additional pipeline stage may be added. It may be desirable to place this additional pipeline stage in the address path, or in the read data path between the memory array and the first intermediate data latch. Other burst length and latency options may be provided as the operating speeds of the device increase, and computer architectures evolve. The device of Figure 1 includes programmability of the address sequence by latching the state of the least significant address bit during a WCBR cycle. The burst length and /CAS latency for this particular embodiment are fixed. Other possible alterations in the feature sets of this DRAM include having a fixed burst mode only, selecting between standard fast page mode (non-EDO) and burst mode, and using the output enable pin (/OE) 42 in combination with /RAS to select between modes of operation. Also, a WCBR refresh cycle could be used to select the mode of operation rather than a control signal in combination with /RAS. A more complex memory device may provide additional modes of operation such as switching between fast page mode, EDO page mode, static column mode and burst operation through the use of various combinations of /WE and /OE at /RAS falling time. One mode from a similar set of modes may be selected through the use of a WCBR cycle using multiple address or data lines to encode the desired mode. Alternately, a device with multiple modes of operation may have wire bond locations, or programmable fuses which may be used to program the mode of operation of the device.

A preferred embodiment of a sixteen bit wide burst EDO mode DRAM designed in accordance with the teachings of this invention has two column address strobe input pins /CASH and /CASL. For read cycles only one /CAS signal needs to toggle. The second /CAS may remain high or toggle with the other /CAS. During burst read cycles, all sixteen data bits will be driven out of part during a read cycle even if one /CAS remains inactive. In a typical

system application, a microprocessor reads all data bits on a data bus in each read cycle, but may only write certain bytes of data in a write cycle. Allowing one of the /CAS control signals to remain static during read cycles helps to reduce overall power consumption and noise within the system. For burst write access cycles, each of the /CAS signals (CASH and /CASL) acts as a write enable for an eight bit width of the data. The two /CAS's are combined in an AND function to provide a single internal /CAS which will go low when the first external /CAS falls, and returns high after the last external /CAS goes high. All sixteen data inputs are latched when the first of the /CAS signals transitions low. If only one /CAS signal transitions low, then the eight bits of data associated with the /CAS that remained high are not stored in the memory.

The present invention has been described with reference to several preferred embodiments. Just as fast page mode DRAMs and EDO DRAMs are available in numerous configurations including x1, x4, x8 and x16 data widths, and 1 Megabit, 4 Megabit, 16 Megabit and 64 Megabit densities; the memory device of the present invention may take the form of many different memory organizations. It is believed that one who is skilled in the art of integrated circuit memory design can, with the aide of this specification design a variety of memory devices which do not depart from the spirit of this invention. It is therefore believed that detailed descriptions of the various memory device organizations applicable to this invention are not necessary.

Figure 3 shows a preferred pinout for the device of Figure 1. It should be noted that the pinout for this new burst EDO memory device is identical to the pinout for a standard EDO DRAM. The common pinout allows this new device to be used in existing memory designs with minimum design changes. The common pinout also allows for ease of new designs by those of skill in the art who are familiar with the standard EDO DRAM pinout. Variations of the described invention which maintain the standard EDO DRAM pinout include driving the /CAS pin with a system clock signal to synchronize data access of the memory device with the system clock. For this embodiment, it may be desirable to use the first /CAS active edge after /RAS falls to latch the

row address, a later edge may be used to latch the first column address of a burst access cycle. After row and column addresses are latched within the device, the address may be incremented internally to provide burst access cycles in synchronization with the system clock. Other pin function alternatives include driving the burst address incrementing signal on the /OE pin since the part does not require a data output disable function on this pin. Other alternate uses of the /OE pin also allow the device to maintain the standard EDO pinout, but provide increased functionality such as burst mode access. The /OE pin may be used to signal the presence of a valid column starting address, or to terminate a burst access. Each of these embodiments provides for a high speed burst access memory device which may be used in current memory systems with a minimum amount of redesign.

Figure 4 is a timing diagram for performing a burst read followed by a burst write of the device of Figure 1. In Figure 4, a row address is latched by the /RAS signal. /WE is low when /RAS falls for an embodiment of the design where the state of the /WE pin is used to specify a burst access cycle at /RAS time. Next, /CAS is driven low with /WE high to initiate a burst read access, and the column address is latched. The data out signals (DQ's) are not driven in the first /CAS cycle, however the data is latched in the intermediate data latch once it becomes valid internally. On the second falling edge of the /CAS signal, the internal address generation circuitry advances the column address and begins another access of the array, and the first data out is latched in the output latch and driven from the device within a /CAS to data access time (tCAC). Additional burst access cycles continue, for a device with a specified burst length of four, until the fifth falling edge of /CAS which latches a new column address for a new burst read access. /WE falling in the fifth /CAS cycle terminates the burst access, and initializes the device for additional burst accesses. The sixth falling edge of /CAS with /WE low is used to latch a new burst address, latch input data and begin a burst write access of the device. Additional input data values are latched on successive /CAS falling edges until /RAS rises to terminate the burst access.

Figure 5 is a timing diagram depicting burst write access cycles

followed by burst read cycles. As in Figure 4, the /RAS signal is used to latch the row address. The first /CAS falling edge in combination with /WE low begins a burst write access with the first data being latched. Additional data values are latched with successive /CAS falling edges, and the memory address is advanced internal to the device in either an interleaved or sequential manner. On the fifth /CAS falling edge a new column address and associated write data are latched. The burst write access cycles continue until the /WE signal goes high in the sixth /CAS cycle. The transition of the /WE signal terminates the burst write access. The seventh /CAS low transition latches a new column address and begins a burst read access (/WE is high). The burst read continues until /RAS rises terminating the burst cycles.

It should be noted from Figure's 3 and 4, that for burst read cycles the data remains valid on the device outputs as long as the /OE pin is low, except for brief periods of data transition. Also, since the /WE pin is low prior to or when /CAS falls, the data input/output lines are not driven from the part during write cycles, and the /OE pin is a "don't care". Only the /CAS signal and the data signals toggle at relatively high frequency, and no control signals other than /CAS are required to be in an active or inactive state for one /CAS cycle time or less. This is in contrast to SDRAMs which often require row address strobes, column address strobes, data mask, and read/write control signals to be valid for one clock cycle or less for various device functions. Typical DRAMs also allow for the column address to propagate through to the array to begin a data access prior to /CAS falling. This is done to provide fast data access from /CAS falling if the address has been valid for a sufficient period of time prior to /CAS falling for the data to have been accessed from the array. In these designs an address transition detection circuit is used to restart the memory access if the column address changes prior to /CAS falling. In a preferred embodiment of the design, the address counter is advanced on /CAS rising edges, and the address generated in the counter is then presented to the array on the next /CAS falling edge when the device is in a burst access mode.

Pipelined Output Buffer

Figure 6 is a schematic representation of an output buffer circuit which has both the intermediate data latch and the output data latch. Complimentary internal data signals 50 and 52 from the memory array are latched in intermediate data latch 54 when valid levels are present during a read cycle. The latched data from the intermediate latch may be multiplexed with the unlatched data signals in multiplexers 56 and 58. The unlatched data signals are selected for /CAS latencies equal to one, and for normal EDO page mode operation. For /CAS latencies greater than one, the select logic 60 will select the latched data to pass through the multiplexers to output data latch 62. The select logic may also deselect all inputs to the multiplexers while the output is latched, or in a high impedance state. This may be done for periods of time when the part is not in a read mode, for brief periods of time between read cycles to reduce or eliminate crossing current in the output buffer, or for maintaining the output data through a read cycle. Pullup and pulldown signals 64 and 66 respectively from the output data latch drive output driver 68 which drives a data signal 70 from the device. The latch control circuit 72 controls whether the latch will be cleared (device data outputs in high impedance state), latched, or open to receive data from the multiplexers.

Figure 7 is a more detailed schematic diagram of one embodiment of the output buffer circuit of Figure 6. While Figure 7 shows considerably more detail than Figure 6, it is not intended to be a complete description of all circuit elements that may be present in an output buffer circuit designed in accordance with the teachings of the present invention. The output driver portion 68 for example shows only two control inputs, and two n-channel transistors. Typical output driver circuits are considerably more complex and may include methods to drive full Vcc levels from the device through n-channel output transistors. Numerous semiconductor device output driver circuits are known to those of skill in the art, and therefore it is not deemed necessary to show such detail in this description.

In Figure 7, complimentary internal data signals D 50 and D* 52 from the memory array are latched in intermediate data latch 54 when valid levels

are present during a read cycle. Between read cycles, signals D and D* are driven inactive low. While D and D* are low, the intermediate data latch will maintain its state. When one of the D and D* signals transitions high, the latch will be set or reset. Once the latch is set or reset, D and D* are returned to their low states in preparation for further access cycles. In this particular embodiment, a NOR type intermediate data latch is used. It is equally useful to utilize a NAND type intermediate data latch where D and D* are inactive high, and the latch is triggered upon D or D* transitioning low.

The latched data from the intermediate latch is multiplexed with the unlatched data signals in multiplexers 56 and 58. Multiplexers 56 and 58 each have two sets of n and p channel transistors. When a multiplexer is enabled, only one selected set of the transistors will be turned on in each multiplexer allowing the signal associated with the selected set of transistors to pass through. For burst access cycles, the select logic 60 selects the latched data to pass through the multiplexers to output data latch 62 whenever the latch control signal LTCH is low indicating that the next data is to be driven from the device. The select logic deselects all inputs to the multiplexers (places the multiplexer outputs in a high impedance state) while LTCH is high holding the output data in the output data latch, or while the output data latch is held in a cleared state. In an alternate embodiment, the LTCH and a clear signal /DOE may be logically combined so that the multiplexers tri-state and the output data latch feedback path is formed whenever the /DOE signal is high. This allows for the output data latch to be cleared in response to the /DOE signal despite the state of the LTCH signal. The /DOE data output enable signal is a clear signal in that it disables the output driver 68 from driving data from the device by clearing the output latch which supplies the output driver control inputs. The select logic circuit shown also has a burst mode signal BURST input for selecting between Burst EDO and normal EDO modes of operation. Pullup and pulldown signals 64 and 66 respectively from the output data latch drive the output driver control inputs of the output driver 68 which drives a data signal 70 from the device. The latch control circuit 72 controls whether the latch will be cleared (device data outputs in high

impedance state), latched, or open to receive data from the multiplexers. In the embodiment of Figure 7, a high level on the /DOE signal will clear the output data latch and tri-state the device output only when then LTCH signal is high. It is possible to design the output data latch such that it is not cleared when the /DOE signal is high in the event that it is deemed desirable drive old data from the output data latch when /DOE transitions low without waiting for /CAS to fall and new data to arrive in the output data latch. Clearing the output data latch allows for the output driver to be maintained in a high impedance state, despite the state of the /DOE signal, until new data is latched in the output data latch by the LTCH signal.

Figure 8 is a timing diagram depicting the operation of the circuit of Figure 7 after a row of the memory device has been selected. A burst read cycle is shown where an initial column address is latched on the first falling edge of /CAS at time t1. A short time after the first column address is latched, data from the selected row and column of the memory device will be valid on the data lines D and D*. Data signals D and D* are inactive and low prior to the selection of the first column address. In response to the first selected column, data signal D transitions high indicating a read access of a logic "1" value. The high transition is latched in the intermediate data latch, and remains at the output of the latch even after the data signal D transitions back to a low level in preparation for the selection of a second column of the memory array.

For a burst access cycle the multiplexers 56 and 58 in Figure 7 select the latched data from the intermediate data latch to pass through to the output data latch whenever the latch control signal LTCH is low and the clear signal /DOE is low. When the LTCH signal is high, the multiplexers are disabled, and data from the output latch is fed back into the output latch circuit. At time t2, LTCH will transition low to allow the data signals from the intermediate data latch to pass into the output data latch in response to the falling edge of /CAS. The first data is then driven from the memory device provided that the /DOE signal is also low. When the LTCH signal transitions back high, the multiplexers are tri-stated, and the output data is latched. The

first data value will remain valid external to the memory device until just after the next falling edge of /CAS at time t3. Since data is valid on the second falling edge of /CAS after the address was latched, the /CAS latency is said to be two. Since valid data is not present in the output data latch between times t1 and t2, the data output enable signal /DOE may remain high until shortly after time t2 when it transitions low allowing the memory device output drivers to drive data from the device. If the LTCH signal is allowed to occur at time t1, then the /DOE signal must be used to hold the outupt driver off in order to prevent invalid data from being driven from the device. A third option is to mask the LTCH pulse that is shown at time t1 since no data is being transferred to the output data latch. In the case of the third option, the output data latch having been cleared by /DOE will remain cleared (output drivers turned off) until the next LTCH pulse at time t2 despite /DOE transitioning low prior to t2. /DOE may also pulse high after each falling edge of /CAS for a very short time to turn off the output drivers while the output data latch is changing states in order to prevent large crossing currents in the output driver which occur when both the output pullup and pulldown transistors are turned on at the same time. In the event that other methods are used to reduce or prevent crossing current in the output driver, the /DOE signal may remain low throughout the burst read access as long as the device /OE pin remains low. In a preferred embodiment of the invention, crossing currents are reduced by delaying the turn on of the pulldown driver until after the pullup driver is turned off. In this preferred embodiment, the /DOE signal transitions high and then low between output data values. The high transition occurs slightly before data is valid at the input to the output data latch allowing the output data to swing towards an intermediate potential. When the LTCH signal transitions low, valid data is rapidly driven through the output data latch to the output driver. The /DOE signal then transitions back low prior to the LTCH signal transitioning high.

Also at time t2, an internal address counter provides a second column address to the memory array, and another read access occurs. This second access may occur while the first data is still being latched in the output data

latch as long as the intermediate data latch does not latch the second data value prior to the first data being latched in the output data latch. A short time after the second /CAS falling edge, D* transitions high indicating a read access of a logic "0" value.

At time t3 a third column is selected, and the second data value is latched in the output data latch and driven from the part. At time t5, a slight dip is shown in the output data signal between valid logic "1" states from the third and fourth data accesses. This dip is the result of the /DOE signal pulsing high to prevent crossing current in the event that the output data signal would be transitioning. If other methods are used, this dip might not appear. One method of preventing crossing currents in the output drivers is taught in U. S. Patent #5,331,593 to Merritt et. al. In a preferred embodiment of the present invention, crossing currents are reduced by preventing the output driver pulldown from turning on prior to the output driver pullup turning off. In this preferred embodiment, the /DOE signal is allowed to pulse high just prior to data valid in order to allow the output to begin to fall in the event that the previous data out is high. Allowing the output to begin to fall prior to data valid speeds up high to low data transitions which helps to compensate for the high to low transition delay introduced in the reduction of crossing currents. Crossing currents could likewise be reduced by preventing the output driver pullup from turning on prior to the output driver pulldown turning off. However, high to low output transitions tend to be faster than low to high output transitions making the first solution more symmetrical.

Address Transition Detection

Figure 9 is block level schematic of a data path portion of the device of Figure 1. In Figure 9, data written to the memory device is received on data I/O pad 100. The write data is passed through input circuit 102 to a global sense amp 82 over write data lines 103. For this example, the sense amplifier includes an I/O line multiplexer 104 which is used to select a path from local I/O data line pair 106 to one of two pairs of array I/O lines 108 and 110. Write data is driven from write data lines 103 to I/O lines 106 when enabled by a logical combination of the equilibrate signal 81 and the write

enable signal 80 from timing circuit 77 and data path control circuit 124 of central logic circuitry 75. In this example array I/O lines 108 are coupled to an adjacent section of the array (not shown). Array I/O lines 110 are true and compliment lines coupled to a local array sense amplifier 112 which is part of array section 79. Column select signal 114 from column driver 115 couples array data I/O lines 110 to a pair of complimentary digit lines 116 inside the local sense amplifier 112. One of the complimentary digit lines is coupled to a memory cell 118 through an access device which is selected by a signal on word line 120 from a row address decoder.

Read data follows the same path from the memory cell to the global sense amp where it is then driven on complimentary data read lines 122 to complimentary data lines 126 under control of data path control logic 124 and timing circuits 77. Output circuit 128 drives data from the memory device in accordance with the mode of operation (burst EDO mode, EDO mode, Fast Page Mode, etc.).

This specific embodiment is not intended to provide an exhaustive description of all forms of the present invention. For example, I/O line multiplexer 104 would not be necessary if there is a global sense amp 83 for each pair of array I/O lines. Alternatively, additional array I/O lines could be multiplexed through the multiplexer 104 to allow for even fewer global sense amplifiers. Another variation is to allow read and write data to share a common path between the global sense amplifiers and the I/O pad. Also, separate input and output data pins can be provided. Numerous additional variations are possible and will be recognized by one of skill in the art.

Figure 10 is a schematic diagram providing additional detail for portions of the circuitry of Figure 9. In Figure 10, /WE and /CAS are logically combined in command latch and control circuit 154. The write command output of circuit 154 is buffered through driver 156 to write command signal line 158. The write command is coupled to a plurality of sense amps 66 through a distributed line resistance represented by resistor 160 over a signal line with distributed capacitive load represented by capacitor 162. Write signal 164 arriving at the sense amplifier will be a delayed

version of the output of the write command from the command latch.

Address inputs 170 are coupled to burst address generator 173 which provides a column address 175 to the memory array. The column address and a version of the write command 176 are used to generate an equilibrate signal 182. Equilibration control signal 182 passes through distributed resistance 184, and is loaded by distributed capacitance 186. A delayed version of the equilibrate signal 188 is coupled to the sense amp 66. Local write driver enable circuit 200 allows write cycle data 103 to be driven for a maximum write cycle time by disabling the write data drivers 240-256 during equilibration of the complimentary data I/O lines 106. The data I/O lines are equilibrated when equilibration device 232 couples the true and compliment lines together in response to the equilibration control signal 222.

For a maximized data write cycle time, the write command 164 can remain active throughout a burst write access. In this case, the write drivers are enabled and disabled by the equilibrate signal which will occur at the beginning of each access cycle. For nonburst mode operation, it is beneficial to provide the write command prior to the end of the equilibrate function to allow the write to begin as soon as possible. For these devices, the write will typically end prior to the next /CAS falling edge to allow the device to meet the column address to data valid access time in (TAA). For EDO devices in particular, the page mode cycle time is very short, but the address access time begins while /CAS is high, so the write cycles should end as soon as possible. One way to allow the write cycle to end as soon as possible is to begin it immediately after the equilibrate is complete.

It is important to note that devices 250 and 256 will generally be enabled simultaneously, as will devices 252 and 254. If the enable gate 212 were not locally present, then the write enable signal would need to be delayed from the equilibrate disable time to guarantee that a current path through devices 250, 232 and 256 or devices 252, 232 and 254 does not exist.

Figure 11 is a schematic diagram of a portion of the column address path of the device of Figure 1 shown generally as block 26. In Figure 11 address 16 is coupled to address buffers 305 and 320 which may be located

within block 26 of Figure 1 or at a remote location of the integrated circuit (near address input pads for example). The output of address buffer 305 is coupled to burst address generator 310. Burst address 330 from the burst address generator is coupled to multiplexer 370 through multiplexer 350 and address lines 360. Multiplexer 370 selects either the buffered address 340 from address buffer 320 or the burst address 360 to be latched in latch 380. Latched column address 390 is coupled to a column address buffer 400 which drives the column address to the column address decoder 30 of Figure 1 to select a column of the memory array. The output of latch 380 is also coupled to an asynchronous address transition detection circuit 420 which generates an equilibration control signal 430 at the beginning of each memory access in response to detected changes in the column address 390. Latched address 390 is also fed back to multiplexer 350. In page mode operation. the multiplexer 370 selects the address from the address buffer 340, and the output of the burst address generator 310 is ignored.

In burst mode. the initial burst address is passed to the latch 370 from the address buffer 340 in response to the first falling /CAS transition. The multiplexer 370 will select the address from address lines 360 for subsequent column addresses within the burst access. The address generator 310 may advance the burst address on rising edges of /CAS. Multiplexer 350 will select the burst address from counter 310 in response to subsequent /CAS falling edges. After an address is latched. the multiplexers 350 and 370 select the address feedback path from 390 through 350. 360 and 370 until the next address is required. This allows the burst address generator to advance on each /CAS rising edge of the burst access.

In an alternate embodiment. the two multiplexers 350 and 370 may be combined into a single multiplexer to select the address from 330, 340 or 390. Another alternative embodiment eliminates the feedback path from address lines 390 to multiplexer 350 while providing additional control of latch 380 to latch the burst address except for a brief period of time after /CAS falls when a new burst address is allowed to pass through.

Figure 12 is an alternate embodiment of the portion of the address path

shown in Figure 11. In Figure 12, elements which have common functions with those of Figure 5 have been given corresponding reference numbers. In Figure 12, a single set of address buffers 320 are coupled to the address counter 310 and multiplexer 355. The latch 380 of Figure 10 is no longer present, and multiplexers 350 and 370 of Figure 10 have been combined into a single multiplexer 355. In page mode operation, the multiplexer 355 selects address lines 340 from the address buffer 320 while /CAS is high. This provides an asynchronous address path from the address buffer to the address transition detection circuit 420 so that the equilibration control signal 430 can be generated for each column address transition while /CAS is high. When /CAS falls, the multiplexer 355 selects feedback path 390 to effectively latch the column address. In burst mode, the initial burst address is passed through the multiplexer 355 in response to the first /CAS falling edge. The initial address is then latched by selecting feedback path 390. The initial address is also loaded into address generator 310 where it may be advanced on rising edges of /CAS. For each subsequent falling edge of /CAS within a burst access, the multiplexer will select lines 330 to provide the next burst address to buffer 400 and address transition detection circuit 420. Then address path 390 is again selected to latch the address which allows the address generator to again advance on the next rising edge of /CAS without disturbing the latched column address 390.

Variations on this embodiment which fall within the scope of the present invention include elimination of the feedback path 390 to the multiplexer in combination with the addition of an address latch between the address buffer 320 and the multiplexer. In this configuration, the latch will store the column address while /CAS is low in page mode, and the address generator will increment in response to falling edges of /CAS eliminating the requirement for a burst address latch or feedback path. The multiplexer may then simply select between a burst address path and a page mode address path. If the address generator is designed to pass the initial burst address from input address 16 through to address lines 330 for each new burst access, then the multiplexer select will only need to be changed when the part is switched

between page mode and burst mode.

Figure 13 is yet another embodiment of the portion of the address path shown in Figure 11. In Figure 13, input address 16 feeds page mode and burst mode address generator 315. In page mode operation, the input address is passed through address generator 315 while /CAS is high, and is latched within address generator while /CAS is low. In burst mode, an initial burst address is passed through the address generator in response to the first /CAS low of the burst access. Subsequent burst addresses are generated within the address generator and passed to address lines 390 on successive /CAS falling edges. Address generator 315 may comprise a counter which advances the burst address on rising /CAS edges, and a latch which drives the burst addresses to lines 390 in response to /CAS falling edges.

Pulse Trapping Circuit

It will be appreciated that the critical timing and minimum pulse width requirement of T_{DTH} on the WE* input can unnecessarily slow the operation of the memory circuit. The elimination of this requirement can be accomplished by including the pulse trapping circuit 500 shown in detail in Figure 14. The pulse trapping circuit operates to latch either a high transition or a low transition in the WE* signal while CAS* is low. The transition which is latched will depend upon the state of the WE* signal when the CAS* signal transitions low. That is, if WE* is high when CAS* goes low, the pulse trapping circuit will look for and latch a low transition in WE*. If WE* is low when CAS* goes low, the pulse trapping circuit will look for and latch a high transition in WE*.

The pulse trapping circuit 500 includes low transition latch 502, high transition latch 504, and a NEW BURST pulse generator 506. The low transition latch 502 is described in detail with reference to Figures 16a, 16b, and 16c. At an initial time when both CAS* and WE* are high, the output of NAND gate 508 (node A_1) would be stabilized at a low logic state (0). The output of NAND gate 510 (Node B_1), therefore, is a high logic state (1). NAND gate 512 in response produces a low output. The outputs of flip-flop 514, Nodes C_1 and D_1, are low and high, respectively. The output, Node E_1,

of the low transition latch 502 will be normally high. When the CAS* signal transitions low, NAND gates 510 and 512 are "enabled". That is, Node B_1 will remain high regardless of the state of Node A_1, and the output of NAND 512 will change to high. With both inputs to flip-flop 514 high, nodes C_1 and D_1 will remain in their prior state. If the WE* signal transitions low while the CAS* signal is low, Node A_1 will latch to a high state and remain at that state even if WE* returns high. When CAS* transitions high, Node B_1 will go low, and Nodes C_1 and D_1 will go high and low, respectively. Delay element 520 will maintain a high output such that both inputs to NAND gate 518 are high. Node E_1, therefore, will pulse low. The length of the pulse is directly dependent upon the length of delay element 520. Thus, low transition latch 502 produces a low pulse if WE* transitions low when CAS* is low. Delay element 521 is included between Node A_1 and NAND gate 516 as a filter for the WE* signal. If WE* pulses low for a time period less than the delay time, Node A_1 will not latch high. This delay therefore reduces the chance that noise on the WE* line will trigger the latch.

The high transition latch 504 is described in detail with reference to Figure 15a, 15b and 15c. In an initial state when CAS* is high and WE* is low, the output (Node A_2) of NOR gate 522 will be stabilized at a high state (1). NAND gate 524 will hold Node B_2 low. Flip-Flop 528 will, therefore, pull Node C_2 high and hold Node D_2 low. When CAS* transitions low, Node B_2 is held high regardless of the state of Node A_2. Both inputs to flip-flop 528 will be high, and Nodes C_2 and D_2 will remain at their prior states. If WE* transitions high while CAS* is low, Node A_2 will latch low and remain there even if WE* returns low. The output of NAND gate 526 will go low when CAS* transitions high. Nodes C_2 and D_2 will, therefore, go low and high, respectively. Delay element 532 will maintain a high output such that both inputs to NAND gate 530 are high. Node E_2, therefore, will pulse low. The length of the pulse is directly dependent upon the length of delay element 532. Thus, high transition latch 504 produces a low pulse if WE* transitions high when CAS* is low. Delay element 534 is included between NOR gate 536 and NOR gate 522 as a filter for the WE* signal. If WE* pulses high for

a time period less than the delay time, Node A_1 will not latch low. This delay therefore reduces the chance that noise on the WE* line will trigger the latch.

Pulse trapping circuit 500 enables either low transition latch 502 or high transition latch 504 when CAS* goes low. If the enabled latch circuit 502 or 504 detects a transition in the WE* signal a low pulse is produced on Node E when the CAS* signal transitions high. NEW BURST pulse generator 506, shown in Figure 14, is included with the pulse trapping circuit to produce a signal indicating that a new burst access is to be initiated. As stated above, a current burst is to be terminated and a new burst initiated on a CAS* rising transition when the WE* signal transitions states. The NEW BURST signal will pulse high on a CAS* high transition if either E_1 or E_2 are low. That is, if either E_1 or E_2 are low the output of NAND gate 538 will be high. Because the output of NOR gate 540 is normally low, flip-flop 544 will force NEW BURST high via inverter 546. If E_1 and E_2 are high, NEW BURST will remain low. To reset the latch when CAS* goes low, the output of NOR gate 540 pulses high in response to a CAS* low transition. The high pulse length is dictated by delay element 542.

Figure 17 illustrates the operation of the pulse trapping circuit. On the first CAS* falling edge WE* is high. The low transition latch 502 latches a low pulse such that NEW BURST goes high on the rising edge of CAS*. The current burst operation is terminated and a new burst read is initiated. NEW BURST will return low on the falling edge of CAS* and remain low until the third rising edge of CAS*. The short pulse on WE* is filtered by delay element 521 and NEW BURST is not pulsed. The third CAS* rising edge terminates the burst read operation and initiates a burst write operation. The fourth CAS* falling edge enables the high transition latch circuit 504. A NEW BURST high pulse is produced on the next CAS* rising edge in response to the WE* high pulse. Again, the short WE* pulse is filtered by delay element 534 such that noise on the WE* line does not trigger the latch. Further, if WE* transitions while CAS* is high a NEW BURST signal will be immediately produced, as illustrated in Figure 17. This provides a direct control of new memory access burst without waiting for a CAS* low

transition.

Figure 18 is a schematic representation of a data processing apparatus designed in accordance with the present invention. For the purposes of this specification a microprocessor may be, but is not limited to, a central processing unit (CPU), a microprocessor, a microcontroller, a digital signal processor, or an arithmetic processor. In Figure 18, microprocessor 112 is connected via address lines 114 and control lines 116 to a memory control circuit 118. The memory control circuit provides address and control signals on lines 122 and 120 respectively to a burst access memory device 124. The burst access memory device sends and receives data over data bus 126. Optional data bus buffer 130 between memory data bus 126 and microprocessor data bus 128 allows for amplification of the data signals, and/or synchronization with the microprocessor and memory control signals. A fast static random access memory (SRAM) cache circuit 132 is also optional and provides higher speed access to data stored in the cache from the memory circuit or the microprocessor. Memory control circuit 118 may be incorporated within the microprocessor. The memory control circuit provides the required address strobe signals and read/write control signals required for burst mode access of the memory circuit. By providing burst access of the memory by the processor, a computer with relatively high memory bandwidth can be designed without the requirement of a fast SRAM cache. SRAMs which are fast enough to provide memory access without wait states can significantly add to the cost of a computer. Thus the burst access memory device of the present invention allows for medium to high performance computers to be manufactured at a cost which is significantly less than those manufactured today. Use of the burst access memory device of the present invention in cooperation with a fast SRAM cache allows for an even higher performance computer design by providing fast access to main memory in the event of a cache miss.

In a burst write operation, the processor 112 provides an initial address and a write command to the memory controller. The memory controller provides a row address to the memory with a row address strobe. The

memory controller then provides a write command, a column address and a column address strobe to the memory. The memory will equilibrate internal data I/O lines in response to receipt of the write command and column address. During the equilibrate operation, write data and write command signals are passed to global sense amplifiers within the burst access memory device. At the end of the equilibrate operation, write data drivers are enabled, and write data is stored in the memory array. In a preferred embodiment, positive (low to high) transitions of /CAS will cause an internal address counter of the memory device to advance to the next burst address. Negative (high to low) transitions of /CAS will then end the previous write cycle, and pass the burst address to the address transition detection circuit which will generate an equilibrate signal to equilibrate the I/O lines. The negative transition of /CAS will also allow the burst address from the counter to select a column of the array. Once the equilibration is complete, the next write will be performed at the burst address from the counter. In an alternate embodiment, a clock signal is input to a burst access device to control generation of a burst address from the counter (SDRAMs for example have a clock input pin).

In a burst read operation, the processor 112 provides an initial address and a read command to the memory controller. The memory controller provides a row address to the memory with a row address strobe. The memory controller then provides a read command, a column address and a column address strobe to the memory. The memory will equilibrate internal data I/O lines in response to receipt of the read command and column address. At the end of the equilibrate operation, data from the specified column of the array will be amplified and driven on the data I/O lines to the output buffer. In a preferred embodiment, positive (low to high) transitions of /CAS will cause an internal address counter of the memory device to advance to the next burst address. Negative (high to low) transitions of /CAS will then allow the burst address to pass to the address transition detection circuit which will generate an equilibrate signal to equilibrate the I/O lines. The negative transition of /CAS will also allow the burst address from the counter to select

a column of the array. Once the equilibration is complete, the next read will be performed at the burst address from the counter. In an alternate embodiment, a clock signal is input to a burst access device to control generation of the burst address within the memory device.

Memory 124 may also operate in a page mode such as Fast Page Mode or EDO mode. Write commands at memory sense amps are enabled by the equilibrate signal becoming inactive at the sense amp. Using the equilibrate signal at the sense amp to gate the write signal to enable the write drivers eliminates wasted time associated with delaying the write driver enable signal to prevent excessive currents from flowing through the write drivers during the equilibration operation. In page mode, the column address is allowed to flow from the microprocessor asynchronously through to the address transition detection circuit while /CAS is high in order to generate an equilibration signal.

Figure 19 is a schematic representation of a single in-line memory module (SIMM) designed in accordance with the present invention. The SIMM has a standard SIMM module pinout for physical compatibility with existing systems and sockets. Functional compatibility with EDO page mode SIMMs is maintained when each of the 2Meg x 8 memory devices 610, 612, 614 and 616 are operated in an EDO page mode. Each of the /CAS signals 618, 620, 622 and 624 control one byte width of the 32 bit data bus 626, 628, 630 and 632. A /RAS 634 signal is used to latch a row address in each of the memory devices, and is used in combination with /WE 636 to select between page mode and burst mode access cycles. Address signals 638 provide a multiplexed row and column address to each memory device on the SIMM. In burst mode, only active /CAS control lines are required to toggle at the operating frequency of the device, or at half the frequency if each edge of the /CAS signal is used as described above. The data lines are required to be switchable at half of the frequency of the /CAS lines or at the same frequency, and the other control and address signals switch at lower frequencies than /CAS and the data lines. As shown in Figure 19, each /CAS signal and each data line is connected to a single memory device allowing for

higher frequency switching than the other control and address signals. Each of the memory devices 610, 612, 614 and 616 is designed in accordance with the present invention allowing for a burst mode of operation providing internal address generation for sequential or interleaved data access from multiple memory address locations with timing relative to the /CAS control lines after a first row and column address are latched.

Figure 20 shows a front view of another SIMM designed in accordance with the present invention. Each device on the SIMM is a 4 Megabit DRAM organized as 1 Meg x 4. In this configuration, a single /CAS controls two memory devices to provide access to a byte width of the data bus. The eight devices shown form a 4 Megabyte SIMM in a 32 bit width. For an 8 Megabyte SIMM in a 32 bit width, there are eight additional devices on the back side (not shown).

Figure 21 shows a preferred pinout for a memory module designed in accordance with the device of Figure 20. This pinout is compatible with pinouts for Fast Page Mode SIMMs and EDO SIMMs. A presence detect pin is provided for indication of EDO operation on pin 66, and in accordance with standard EDO part types, an /OE input is provided on pin 46.

Alternate embodiments of the SIMM modules of Figures 19, 20 and 21 include the use of two /RAS signals with each controlling a sixteen bit width of the data bus in accordance with standard SIMM module pinouts. Four more 2M x 8 EDO Burst Mode DRAMs may be added to the device of Figure 19 to provide for a 4M x 32 bit SIMM. Sixteen bit wide DRAMs may also be used, these will typically have two /CAS signals each of which controls an eight bit data width. The incorporation of parity bits, or error detection and correction circuitry provide other possible SIMM module configurations. Methods of performing error detection and/or correction are well known to those of skill in the art, and detailed descriptions of such circuits are not provided in this application. Additional SIMM designs using the novel memory device of the present invention may be designed by one of skill in the art with the aid of this specification. The invention has been described with reference to SIMM designs, but is not limited to SIMMs. The invention

is equally applicable to other types of memory modules including Dual In-Line Memory Modules (DIMMs) and Multi-Chip Modules (MCMs).

WHAT IS CLAIMED IS:

1. A memory device having a plurality of memory elements, each of the plurality of memory elements having an associated address, the memory device further comprising:

addressing circuitry adapted to receive at least a portion of a first address from a source external to the memory device in response to a transition of an address latch signal, and further adapted to advance the first address in a predetermined address sequence in response to a subsequent transition of the address latch signal; and

output buffer circuitry adapted to drive data from the memory device after a plurality of transitions of the address latch signal in a burst read access.

2. The memory device of claim 1, wherein:

the output buffer circuitry is further adapted to switch between a logic low data value and a logic high data value in response to a single transition of the address latch signal.

3. The memory device of claim 1, wherein:

the output buffer circuitry is further adapted to drive a logic low data value from the memory device after a falling edge of the address latch signal, and then to drive a logic high data value from the memory device after a rising edge of the address latch signal.

4. The memory device of claim 1, 2 or 3, further comprising:

an intermediate data latch electrically interposed between the plurality of memory elements and the output buffer circuitry to store data from the first address prior to the subsequent transition of the address latch signal.

5. The memory device of claim 1, 2 or 3, further comprising:

an intermediate data latch electrically interposed between the plurality of memory elements and the output buffer circuitry to store data from the plurality of memory elements in response to a transition of a data signal.

6. The memory device of claim 1, 2 or 3, wherein the output buffer circuitry comprises:

an output driver circuit having a driver control input; and

an output data latch adapted to receive a latch control signal and a clear signal, the output data latch further adapted to receive an internal data signal and drive the driver control input in response to a first state of a latch control signal, the output data latch further adapted to store the internal data signal and drive the driver control input in response to a second state of the latch control signal and a first state of the clear signal, and the output data latch being cleared in response to the second state of the latch control signal and a second state of the clear signal.

7. The memory device of claim 1, 2 or 3, further comprising:

an address transition detection circuit coupled to the addressing circuitry, the address transition detection circuit having an output coupled to the plurality of memory elements, providing an equilibration signal to the plurality of memory elements in response to the first address in a first mode of operation, and the address transition detection circuit providing an equilibration signal to the plurality of memory elements in response to each address of the predetermined address sequence in a second mode of operation.

8. The memory device of claim 7 further comprising:

a mode select circuit coupled to the addressing circuitry;

a pair of complimentary data lines coupled to the plurality of memory elements; and

an equilibration control device responsive to the equilibration signal to equilibrate the pair of complimentary data lines.

9. The memory device of claim 8, wherein the equilibration control device comprises:

a first multiplexer having a first input, a second input and an output;

a second multiplexer having a first input, a second input and an output, the output of the second multiplexer coupled to the second input of the first multiplexer;

an input address buffer coupled to the first input of the first multiplexer;

an address counter coupled to the first input of the second multiplexer;

an address latch having an input coupled to the output of the first multiplexer, and an output coupled to the second input of the second multiplexer; and

a signal transition detection circuit coupled to the output of the address latch.

10. The memory device of claim 1, 2 or 3, further comprising:

a control signal input for receiving a control signal; and

a signal trapping circuit coupled to the control signal input and the address latch signal and adapted to latch a transition in the control signal, the signal trapping circuit comprises:

a low transition latch circuit to latch a high to low transition in the control signal when the address latch signal is activated, and

a high transition latch circuit to latch a low to high transition in the control signal when the address latch signal is activated.

11. The memory device of claim 10 wherein the signal trapping circuit further comprises:

a pulse generator circuit coupled to the low transition latch circuit and the high transition latch circuit to generate a pulse in response to an output of the low transition latch circuit and the high transition latch circuit.

12. The memory device of claim 10 or 11 wherein:

the low transition latch circuit comprises a latch circuit connected to the control signal input, and an enable circuit connected to the latch circuit to enable the latch circuit in response to an active transition of the address latch signal and the control signal; and

the high transition latch circuit comprises a latch circuit connected to the control signal input, and an enable circuit connected to the latch circuit to enable the latch circuit in response to an active transition of the address latch signal and the control signal.

13. A method of operating a memory device, the memory device having an array of memory elements, where a first one of the memory elements having a first address has been identified and accessed, the method comprising the steps of:

providing an address of a second memory element from within the memory device and then accessing the second memory element in response to a transition of an address latch signal; and

driving data from the memory device after a plurality of transitions of the address latch signal.

14. The method of claim 13 further comprising the steps of:

latching the first address in response to the address latch signal;

accessing a first data value from the array;

latching the first data value in an intermediate data latch;

latching the first data value in an output data latch in response to a subsequent address latch signal; and

accessing a second data value from the array in response to the

subsequent address latch signal.

15. The method of claims 13 or 14 further comprising steps of:

latching the address of the second memory element;

detecting a difference between the addresses of the first and second memory elements; and

generating an equilibration signal in response to the step of detecting a difference.

16. The method of claim 13 further including the step of:

receiving a control signal on a control signal input;

enabling a latch circuit in response to an active transition of the address latch signal; and

latching a transition of the control signal.

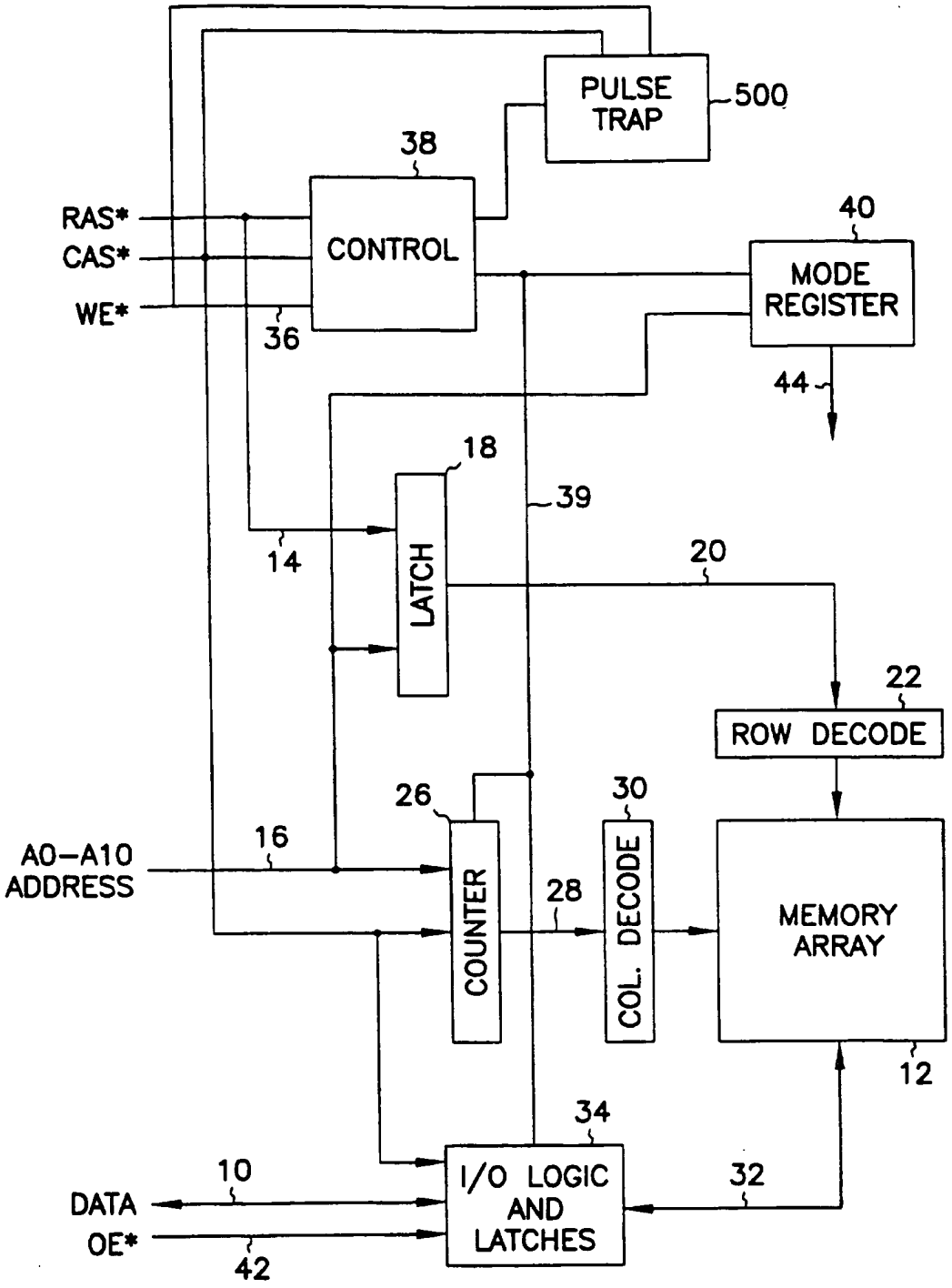

PULSE TRAP
500
38
RAS*
CAS*
WE*
CONTROL
36
40
MODE REGISTER
44
18
39
14
LATCH
20
22
ROW DECODE
26
30
A0–A10 ADDRESS
16
COUNTER
28
COL. DECODE
MEMORY ARRAY
12
34
10
DATA
OE*
42
I/O LOGIC AND LATCHES
32

FIG. 1

Burst Length	Starting Column Address A_2	A_1	A_0	Linear	Interleave
2	V	V	0	0-1	0-1
	V	V	1	1-0	1-0
4	V	0	0	0-1-2-3	0-1-2-3
	V	0	1	1-2-3-0	1-0-3-2
	V	1	0	2-3-0-1	2-3-0-1
	V	1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

FIG. 2

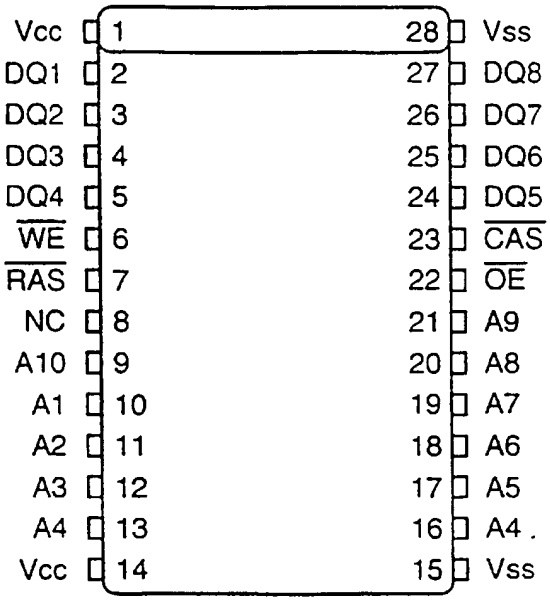

Vcc 1
DQ1 2
DQ2 3
DQ3 4
DQ4 5
WE 6
RAS 7
NC 8
A10 9
A1 10
A2 11
A3 12
A4 13
Vcc 14
28 Vss
27 DQ8
26 DQ7
25 DQ6
24 DQ5
23 CAS
22 OE
21 A9
20 A8
19 A7
18 A6
17 A5
16 A4
15 Vss

FIG. 3

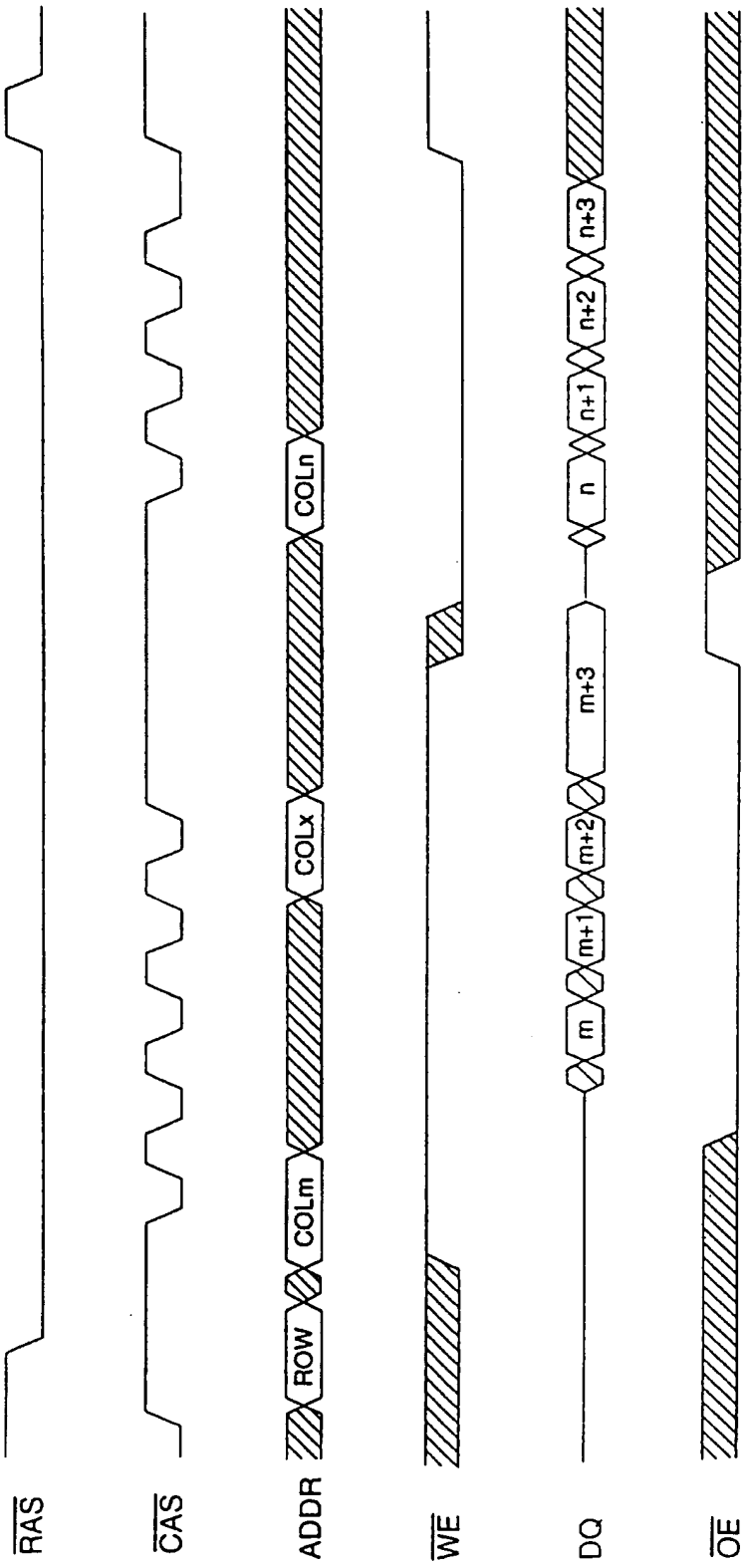


FIG. 4

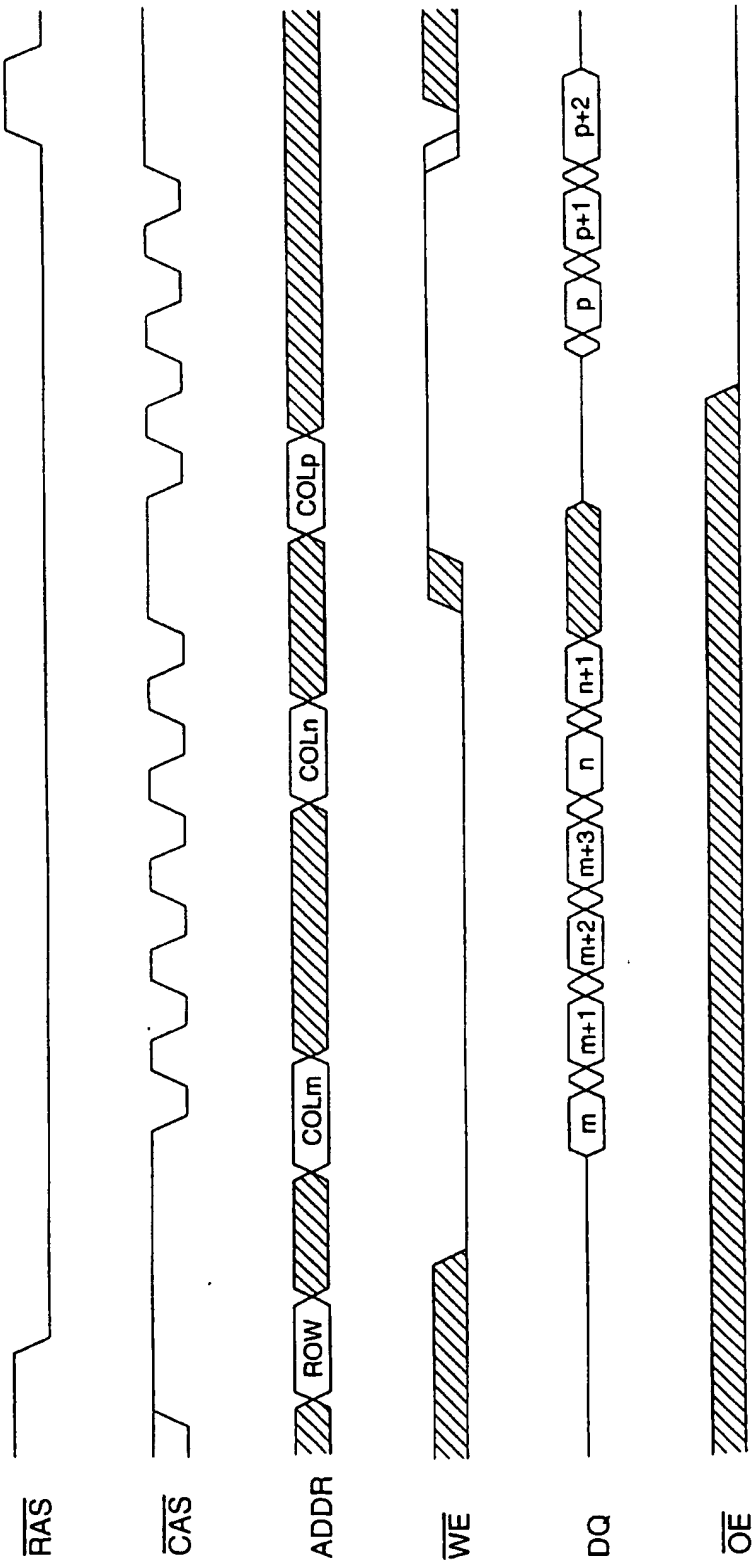


FIG. 5

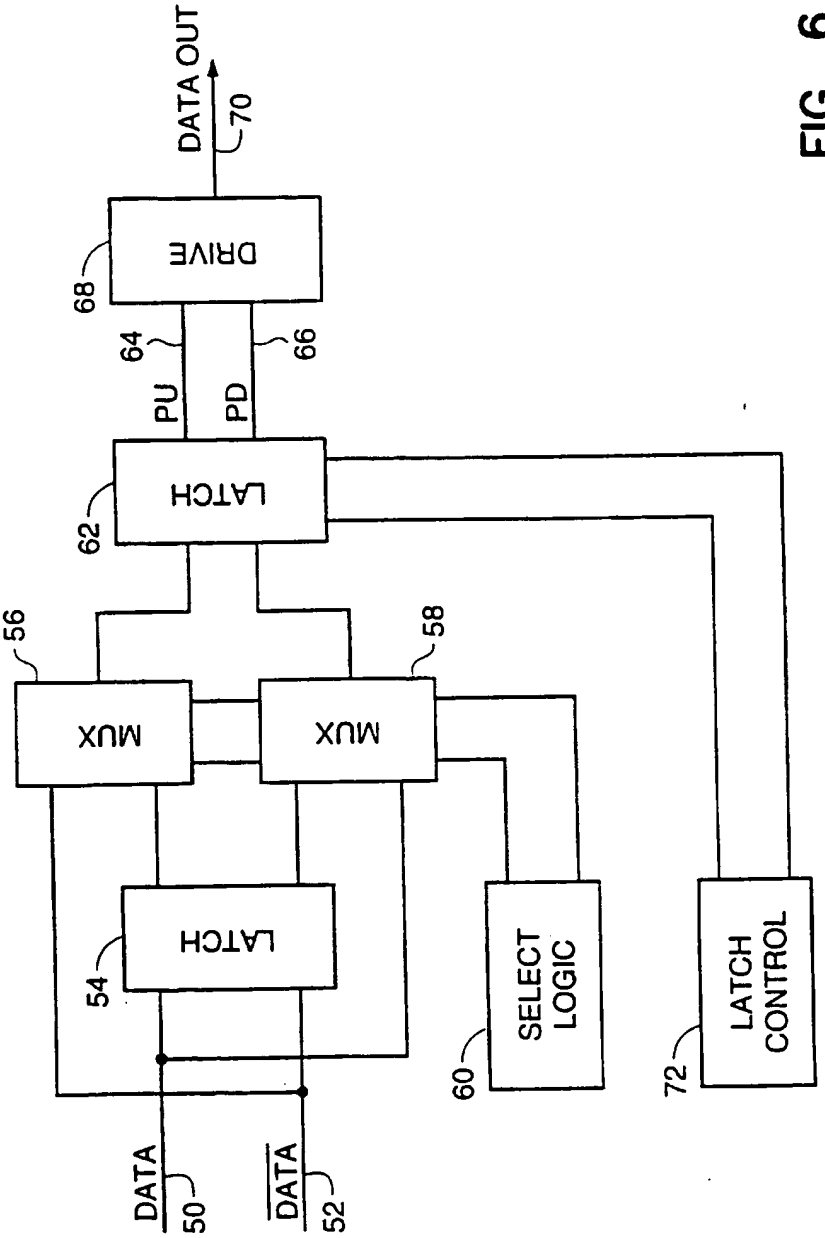

DATA OUT
70
DRIVE
68
64
66
PU
PD
LATCH
62
56
58
MUX
MUX
LATCH
54
SELECT LOGIC
60
LATCH CONTROL
72
DATA
50
DATA
52

FIG. 6

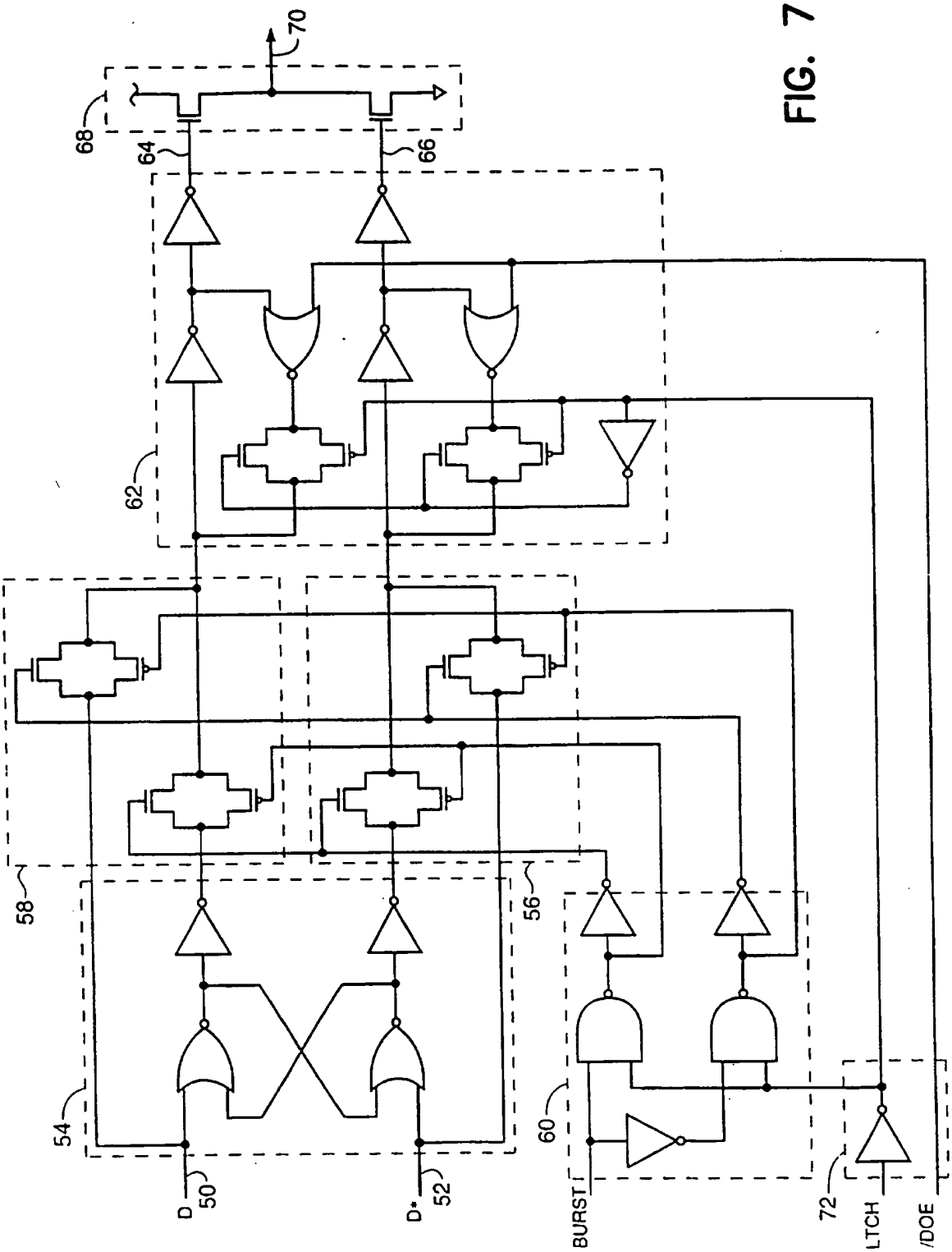


FIG. 7

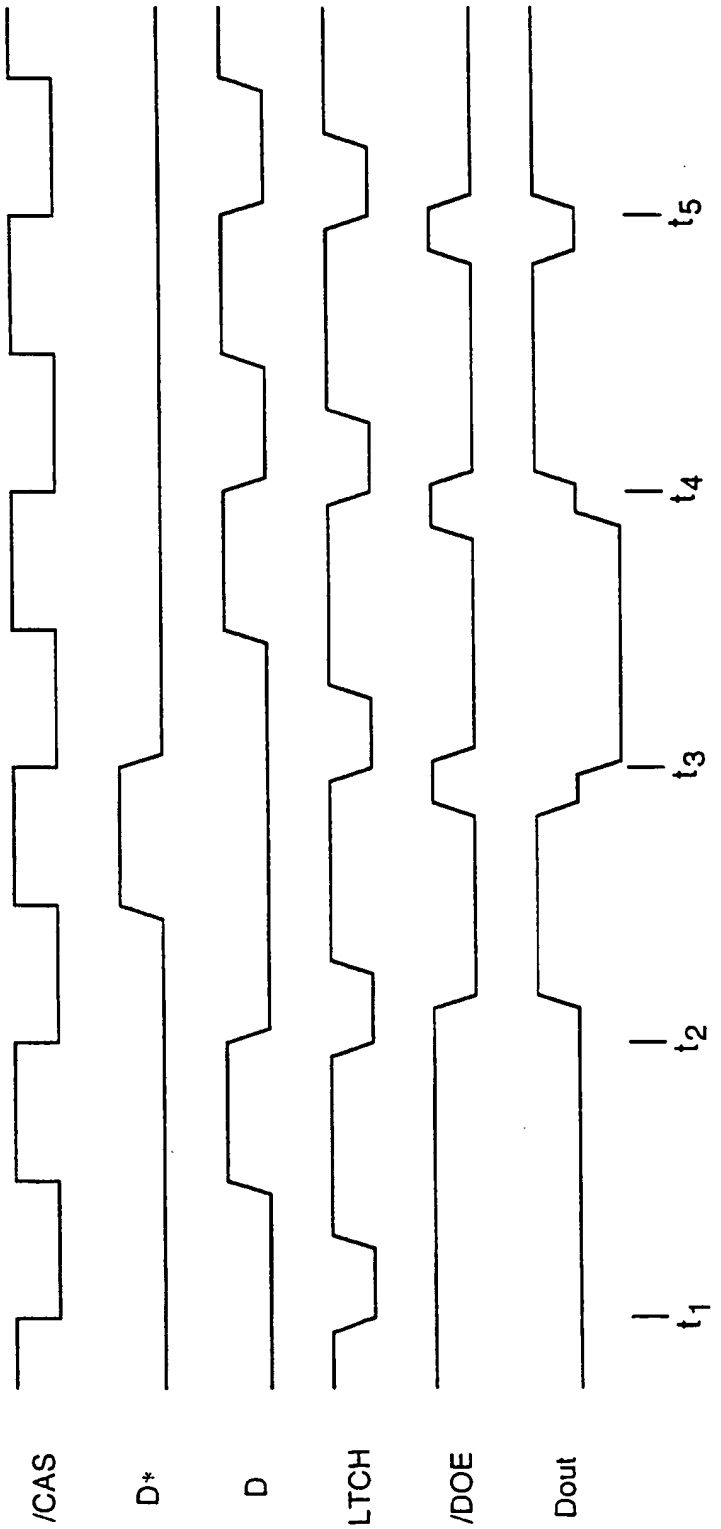


FIG. 8

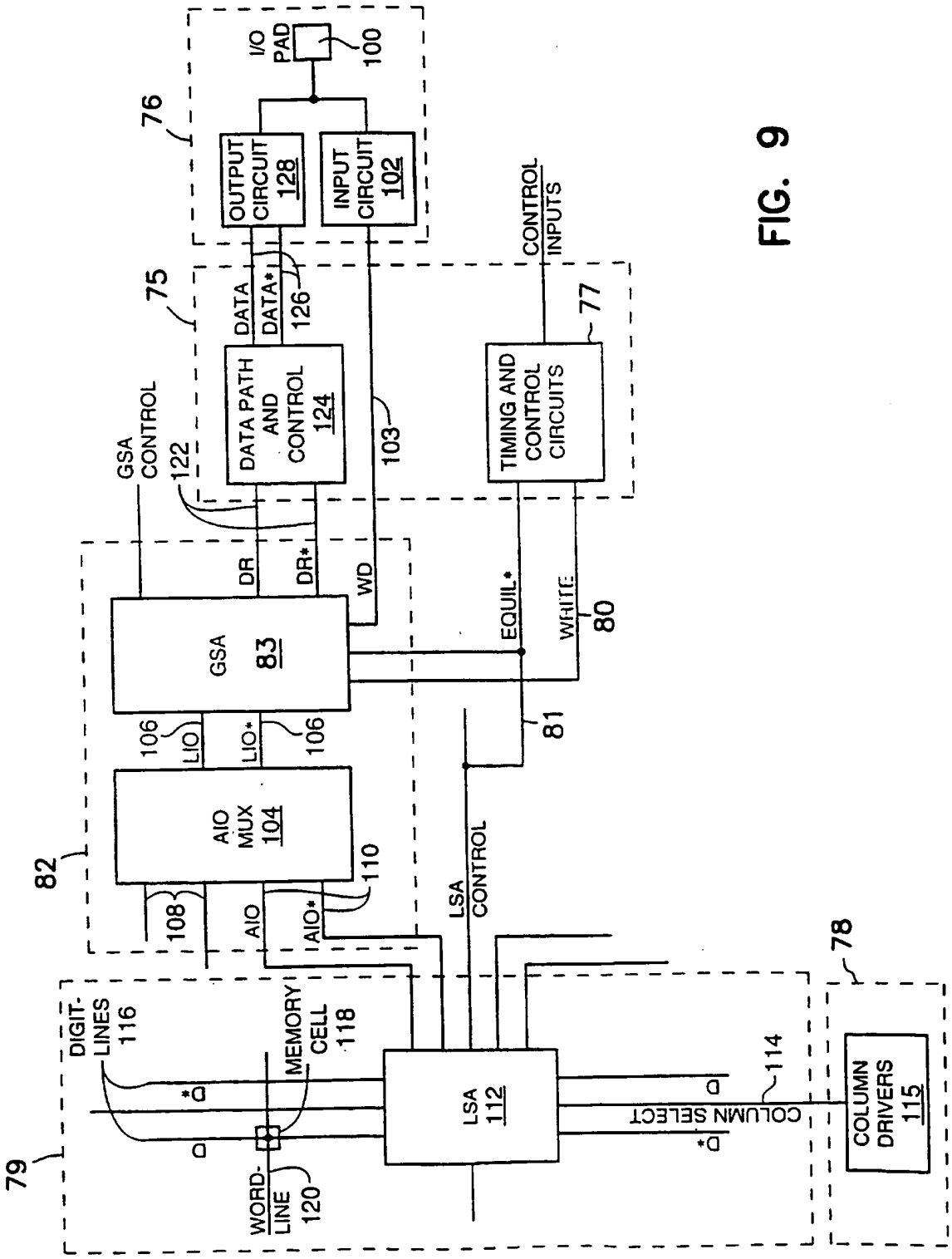

I/O PAD
100
76
OUTPUT CIRCUIT 128
INPUT CIRCUIT 102
CONTROL INPUTS
75
DATA
DATA*
126
77
DATA PATH AND CONTROL 124
TIMING AND CONTROL CIRCUITS
GSA CONTROL
122
103
DR
DR*
WD
EQUIL*
WHITE
80
GSA 83
106
LIO
LIO*
106
81
AIO MUX 104
82
110
108
AIO
AIO*
LSA CONTROL
78
DIGIT-LINES 116
MEMORY CELL 118
LSA 112
114
COLUMN SELECT
COLUMN DRIVERS 115
79
WORD-LINE 120

FIG. 9

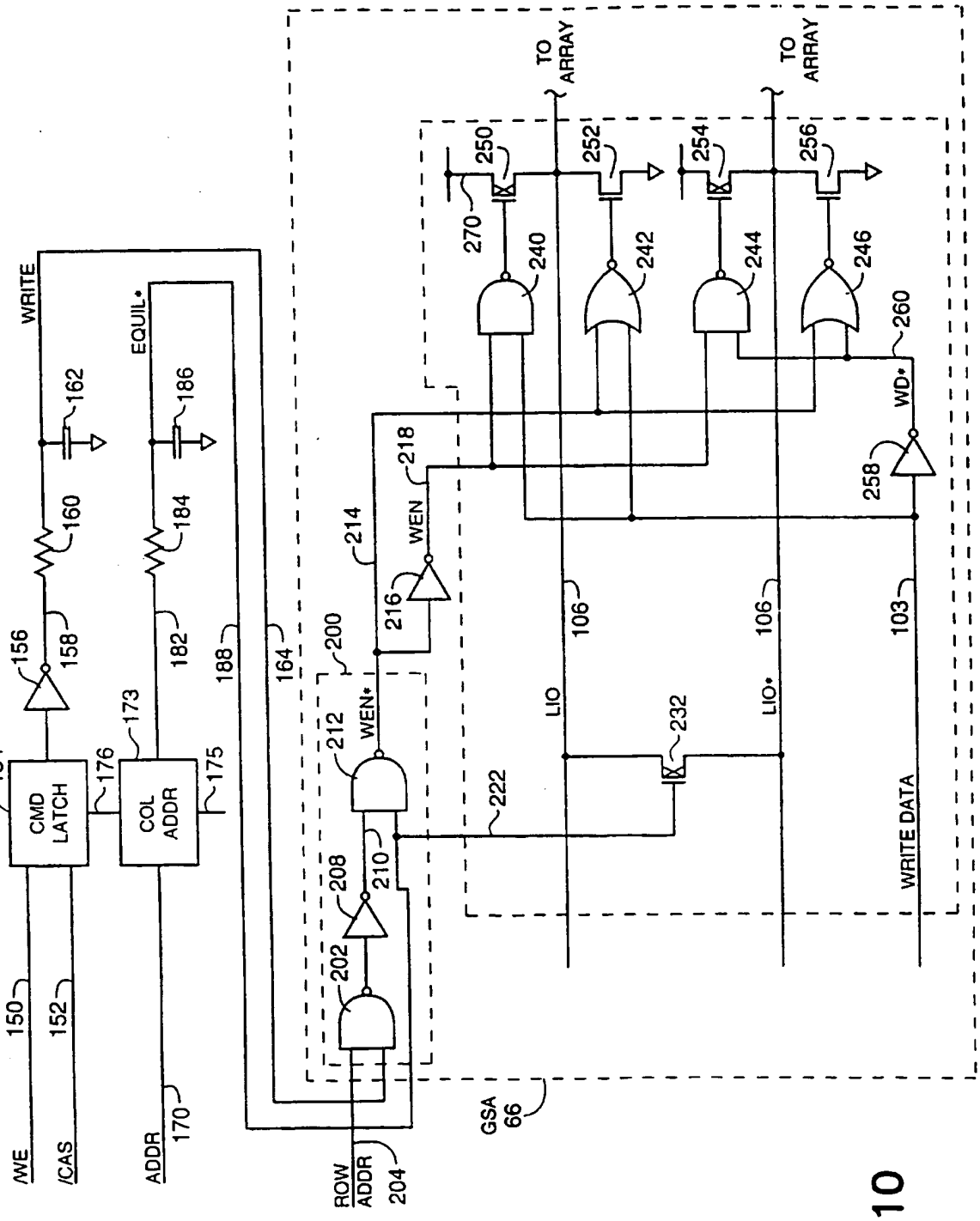

WRITE
EQUIL*
162
186
160
184
156
158
182
188
164
154
CMD LATCH
176
173
COL ADDR
175
150
152
170
/WE
/CAS
ADDR
200
212
WEN*
208
210
202
ROW ADDR
204
214
216
WEN
218
222
GSA 66
106
LIO
232
LIO*
TO ARRAY
TO ARRAY
250
252
254
256
270
240
242
244
246
260
WD*
258
103
WRITE DATA

FIG. 10

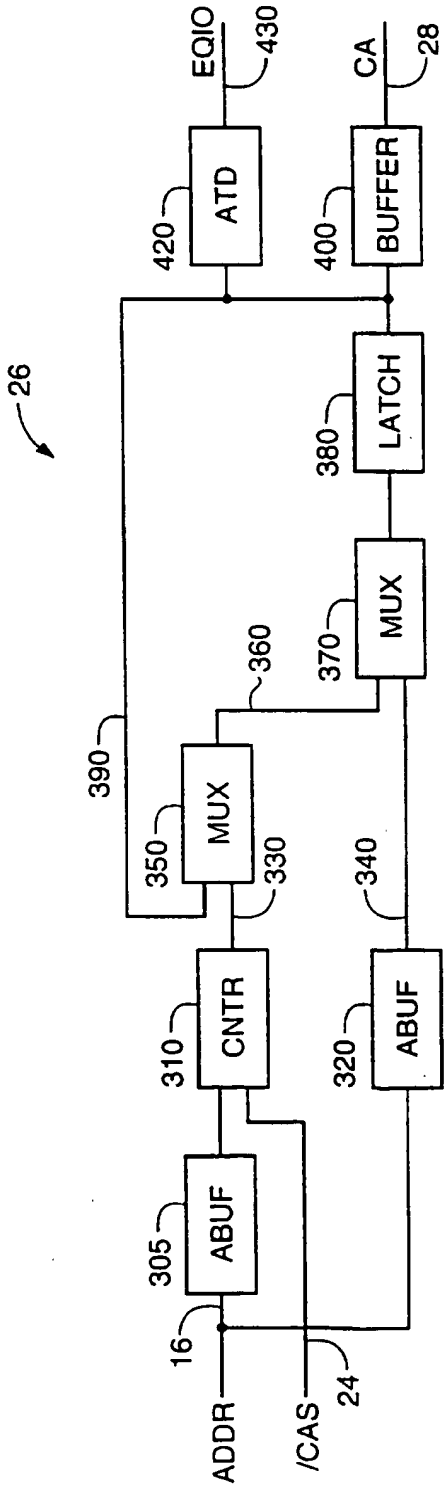

26
EQIO
430
CA
28
ATD
420
BUFFER
400
LATCH
380
MUX
370
360
390
MUX
350
330
340
CNTR
310
ABUF
320
ABUF
305
16
24
ADDR
/CAS

FIG. 11

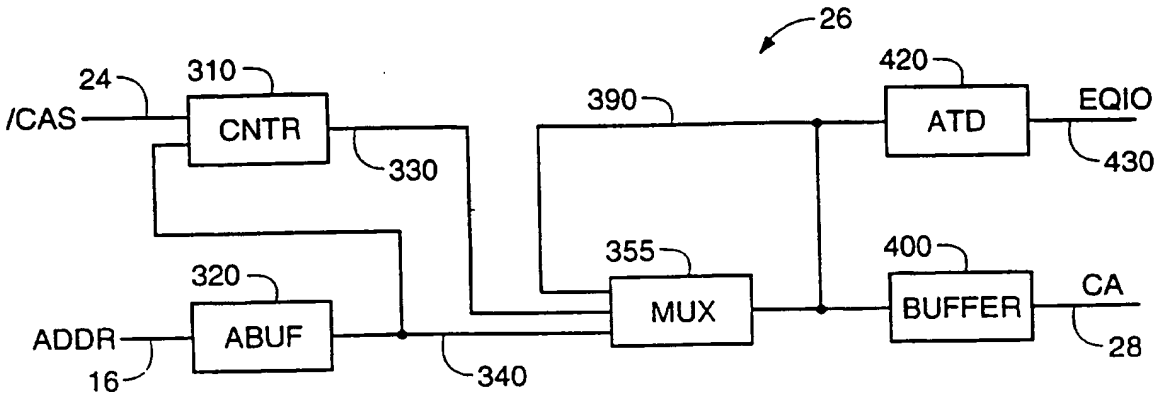

26
24
/CAS
310
CNTR
330
390
420
ATD
EQIO
430
355
MUX
400
BUFFER
CA
28
320
ABUF
ADDR
16
340

FIG. 12

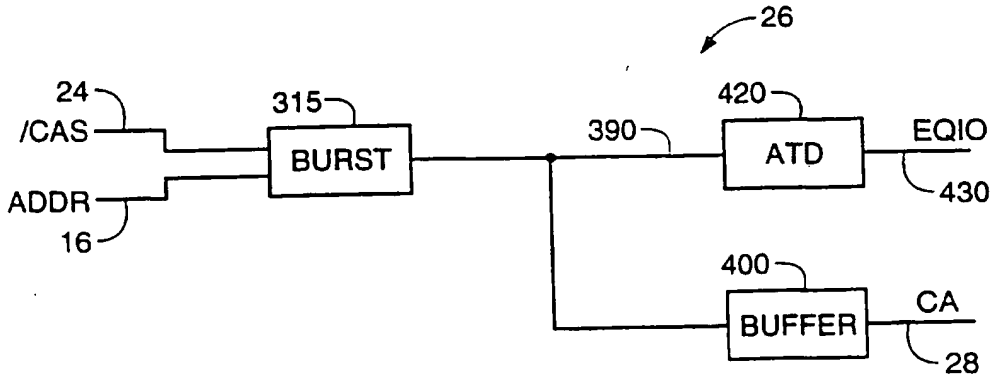
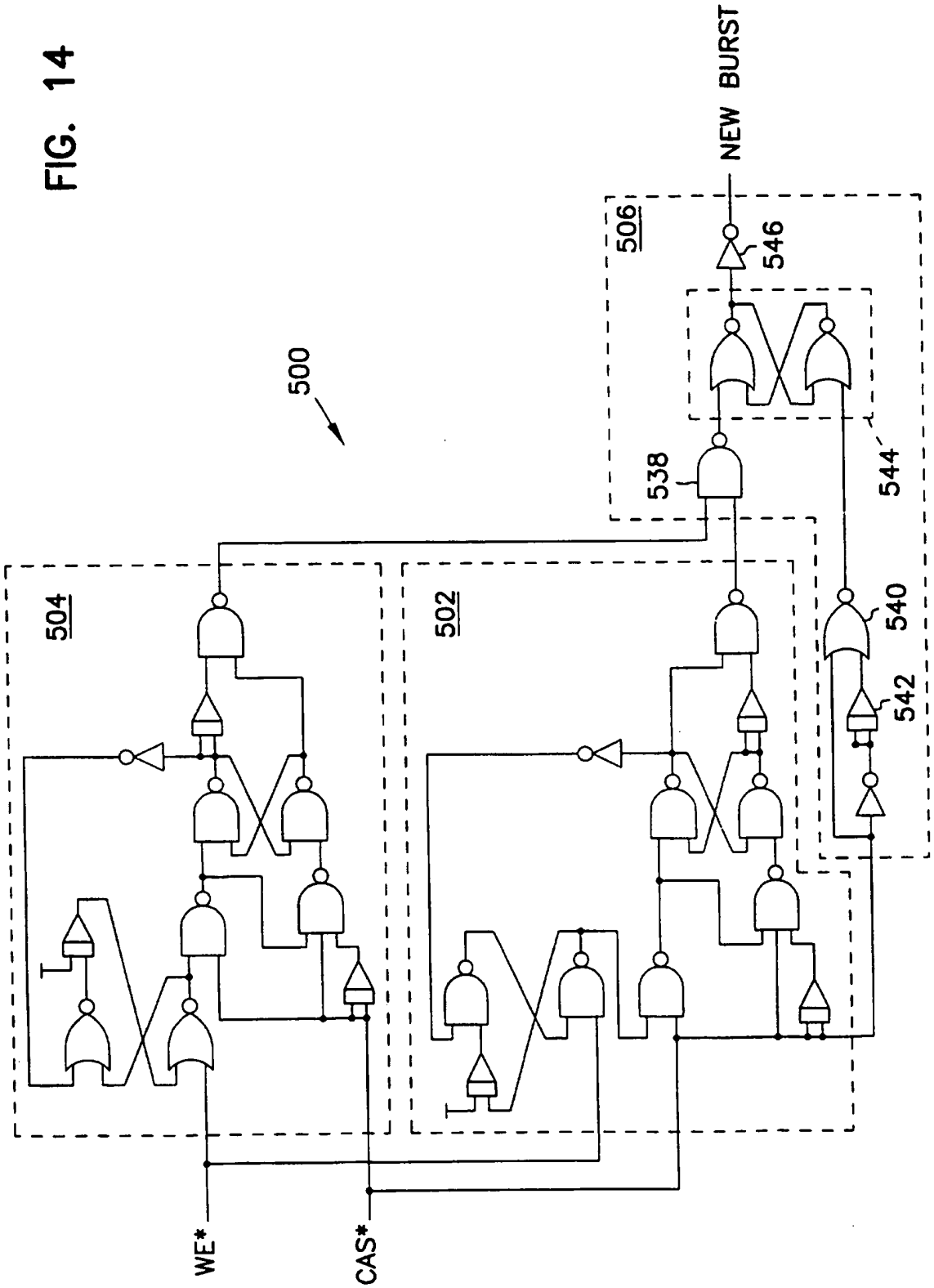

26
24
/CAS
315
BURST
390
420
ATD
EQIO
430
ADDR
16
400
BUFFER
CA
28

FIG. 13

FIG. 14



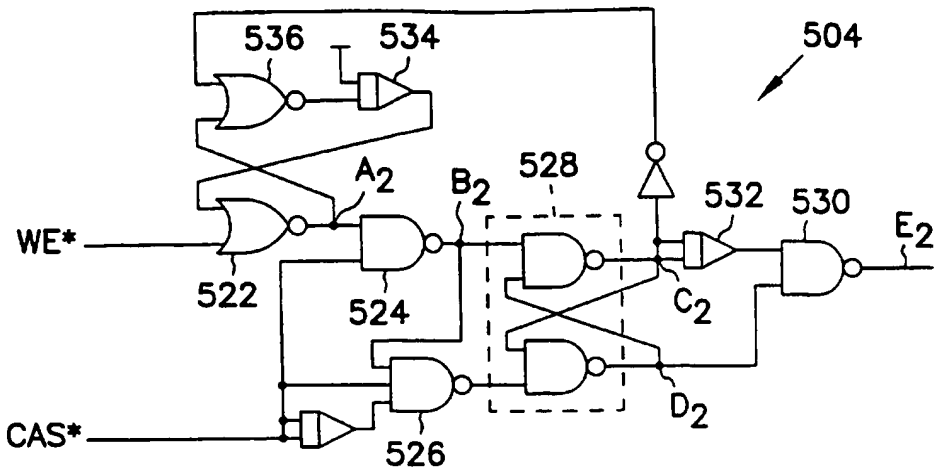


FIG. 15A

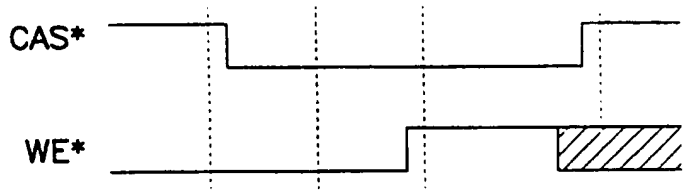


FIG. 15B

	WE* CAS* 0 1	0 0	1 0	X 1
A_2	1	1	0	0
B_2	0	1	1	1
C_2	1	1	1	0
D_2	0	0	0	1
E_2	1	1	1	⊓

FIG. 15C

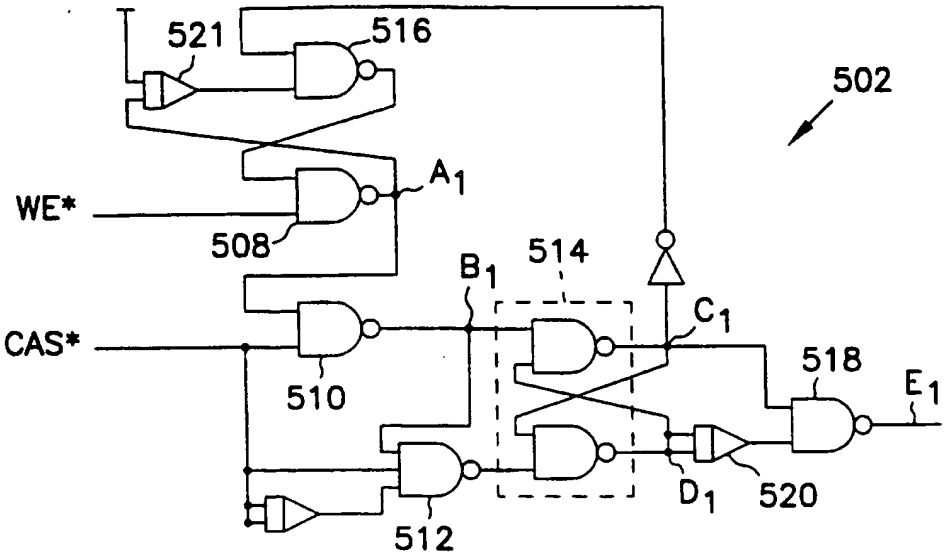


FIG. 16A

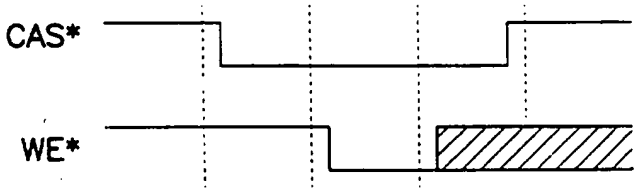


FIG. 16B

	WE* CAS* 1 1	1 0	0 0	X 1
A_1	0	0	1	1
B_1	1	1	1	0
C_1	0	0	0	1
D_1	1	1	1	0
E_1	1	1	1	⊓

FIG. 16C

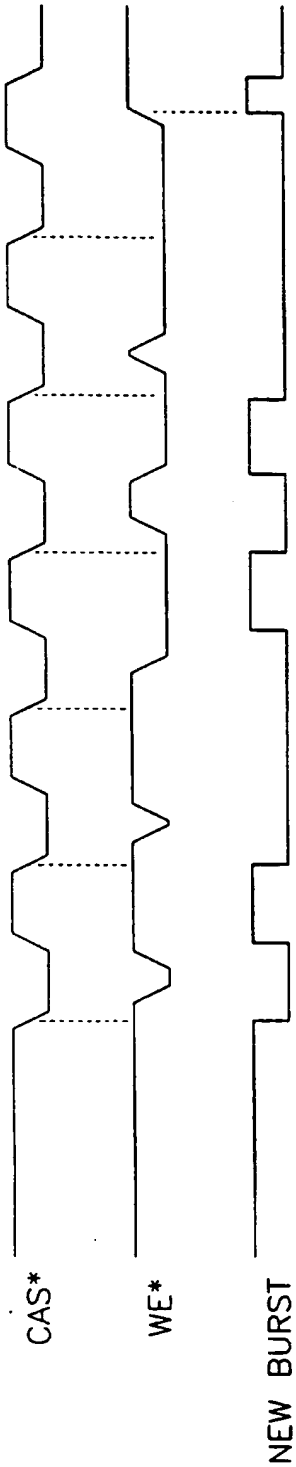


FIG. 17

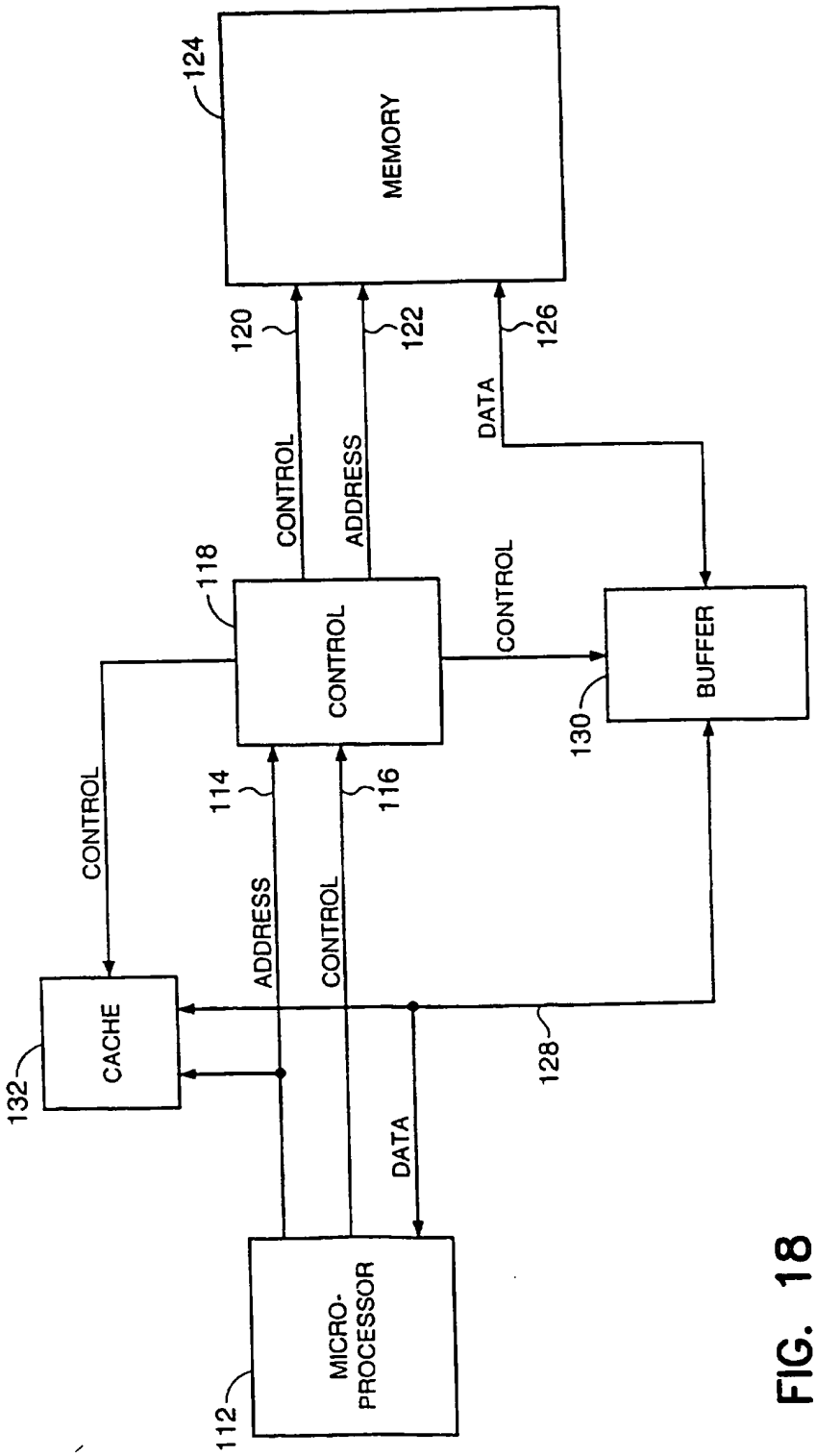

MEMORY
124
120
122
126
DATA
CONTROL
ADDRESS
118
CONTROL
CONTROL
BUFFER
130
CONTROL
114
116
ADDRESS
CONTROL
CACHE
132
128
DATA
MICRO-
PROCESSOR
112

FIG. 18

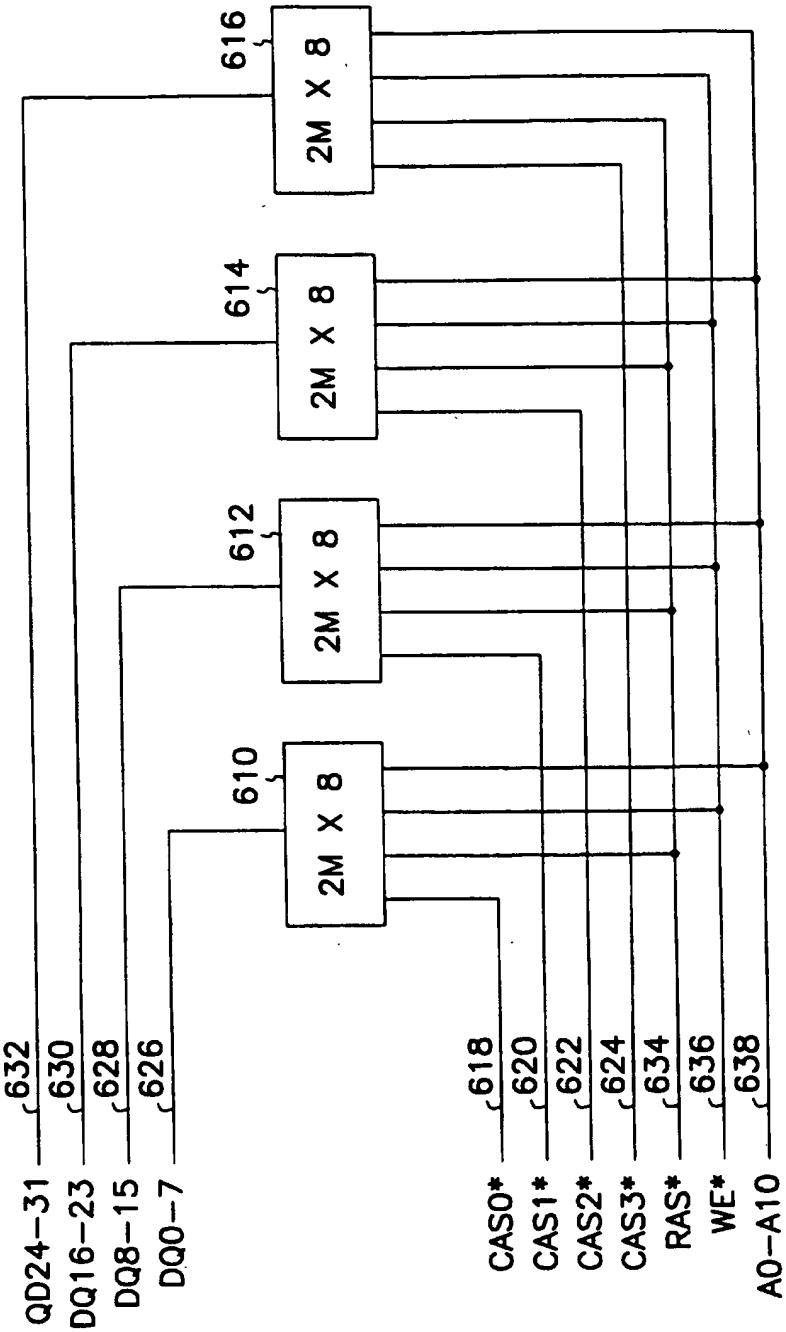

616
614
612
610
2M X 8
2M X 8
2M X 8
2M X 8
632
630
628
626
618
620
622
624
634
636
638
QD24–31
DQ16–23
DQ8–15
DQ0–7
CAS0*
CAS1*
CAS2*
CAS3*
RAS*
WE*
A0–A10

FIG. 19

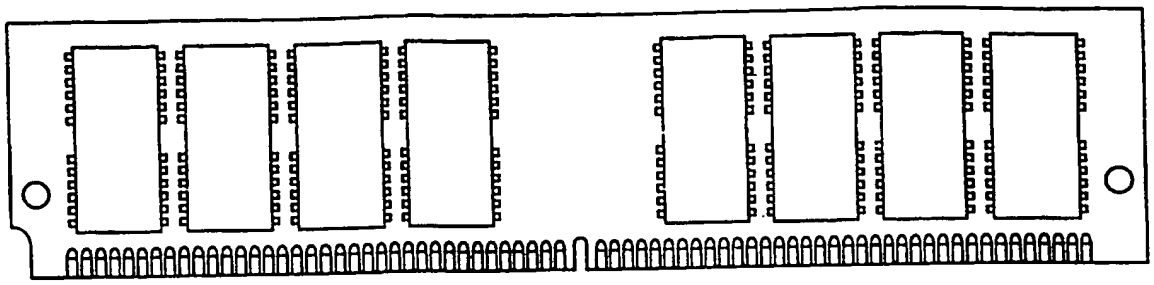


FIG. 20

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	A10	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ29
5	DQ18	23	DQ22	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ30
7	DQ19	25	DQ23	43	$\overline{CAS1}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ31
9	DQ20	27	DQ24	45	$\overline{RAS1}$	63	DQ15
10	Vcc	28	A7	46	$\overline{OE}$	64	DQ32
11	PD5	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	PD ECC	66	PD EDO
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ25	68	PD2
15	A3	33	NC	51	DQ10	69	PD3
16	A4	34	NC	52	DQ26	70	PD4
17	A5	35	NC	53	DQ11	71	PD refresh
18	A6	36	NC	54	DQ27	72	Vss

FIG. 21

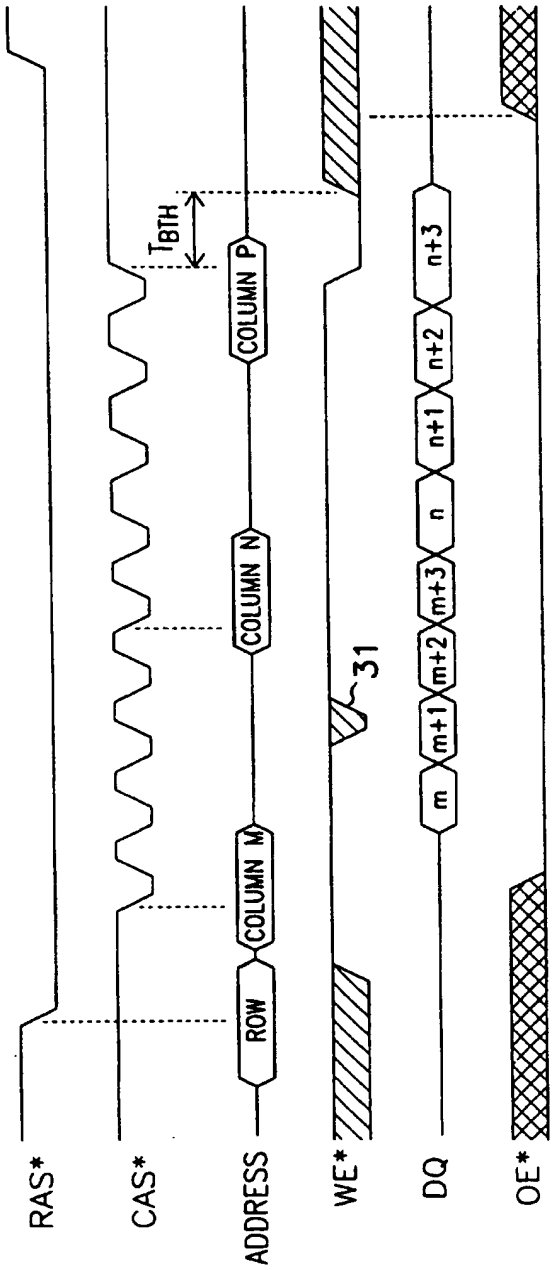

RAS*
CAS*
ADDRESS
WE*
DQ
OE*
ROW
COLUMN M
COLUMN N
COLUMN P
T_{BTH}
31
m
m+1
m+2
m+3
n
n+1
n+2
n+3

FIG. 22

INTERNATIONAL SEARCH REPORT

International lication No
PCT/US 95/16984

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G11C7/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	ELECTRONIC ENGINEERING, vol. 66, no. 813, September 1994, LONDON GB, pages 47-48, XP000445400 "HYPER PAGE MODE DRAM" see the whole document ---	1,13
A	IEEE 1992 CUSTOM INTEGRATED CIRCUITS CONFERENCE, May 1992, BOSTON USA, pages 781-784, XP000340865 GOWNI ET AL.: "A 9NS, 32K x 9, BCMOS TTL, SYNCHRONOUS CACHE RAM WITH BURST MODE ACCESS" see the whole document --- -/--	1,13

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 May 1996	14.06.96

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax (+ 31-70) 340-3016	Stecchina, A

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INTERNATIONAL SEARCH REPORT

International 'ication No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	ELECTRONIC DESIGN, vol. 41, no. 15, July 1993, HASBROUCK HEIGHTS, NEW JERSEY US, pages 55-70, XP000387992 BURSKY: "NOVEL I/O OPTIONS AND INNOVATIVE ARCHITECTURES LET DRAMS ACHIEVE SRAM PERFORMANCE" see page 55, left-hand column, line 1 - page 56, right-hand column, line 11; figure 1 ---	1,13
A	US,A,5 280 594 (YOUNG ET AL.) 18 January 1994 see abstract see column 3, line 27 - column 5, line 34; figure 4 -----	1,13

1

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International ication No
PCT/US 95/16984

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A-5280594	18-01-94	NONE	

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